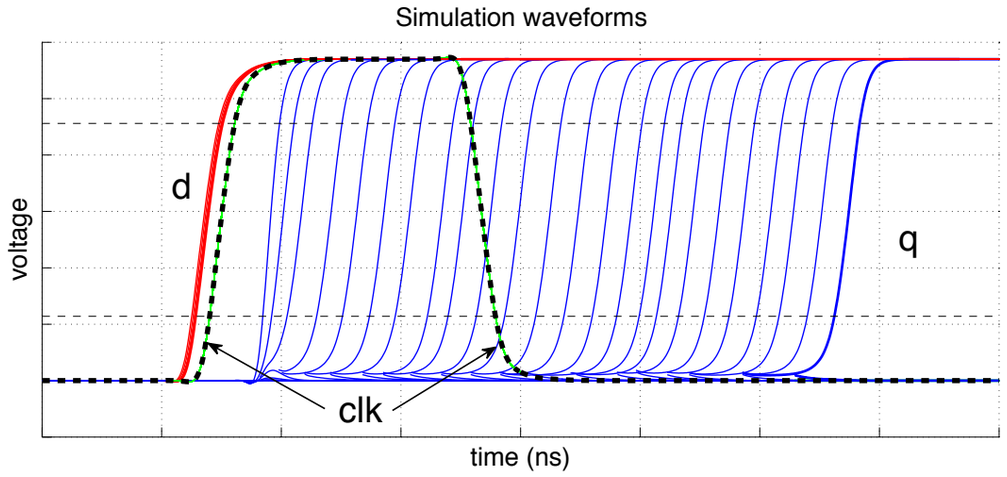
SIMMAT

A Metastability Analysis Tool



Ian W. Jones and Suwen Yang,
Oracle Labs,
Mark Greenstreet,
University of British Columbia

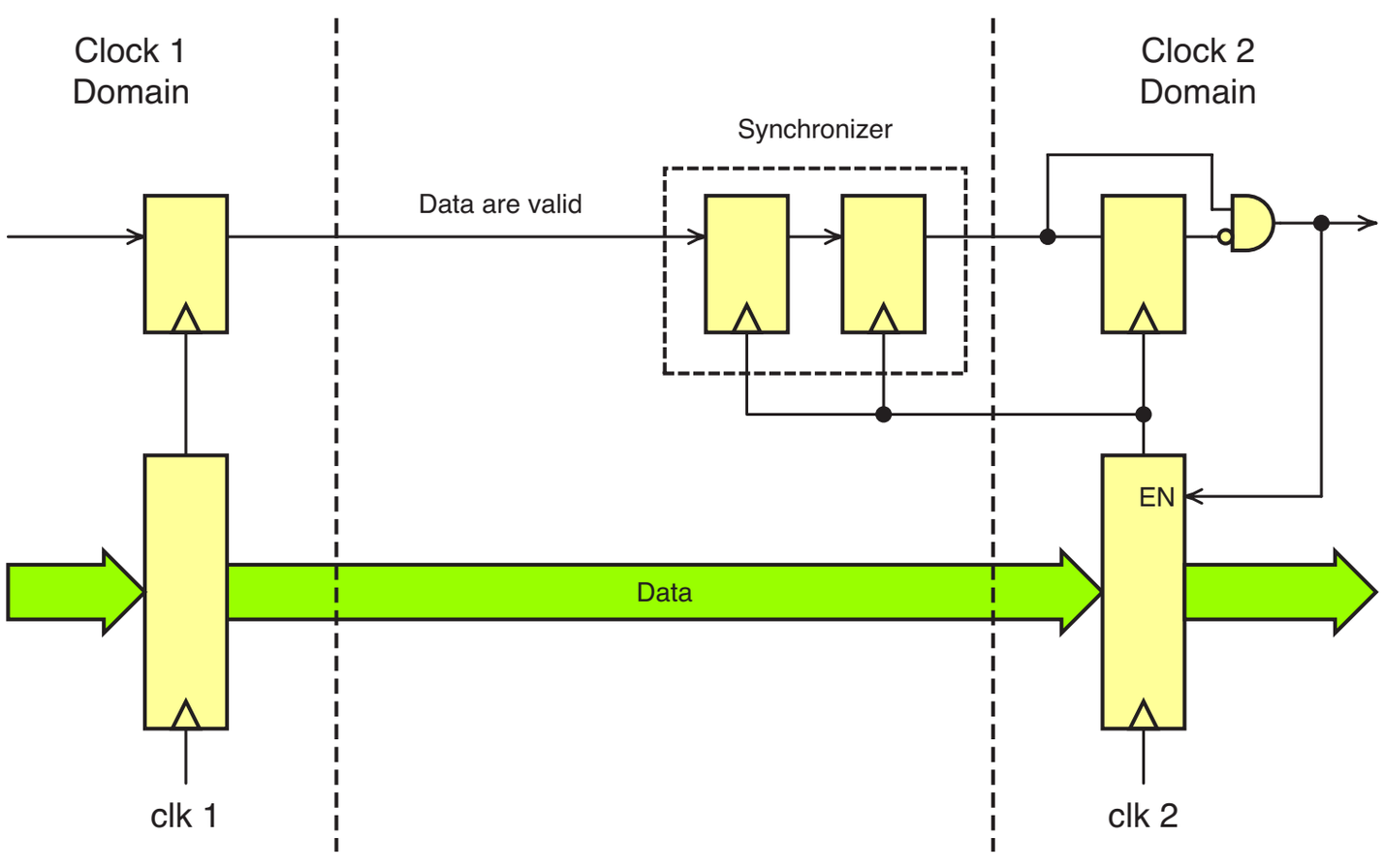
1 November 2012

Outline

- Introduction and Motivation
- Synchronizer behaviors
- Metastability analysis using SIMMAT
- Video animation of SIMMAT
- Conclusion

Introduction

- Multiple independent clock domains on processor chips
- Synchronizers employed to ensure reliable data transfers between clock domains



Motivation

- Modern processors in sub-micron processes:
  - multiple clock domains, 100's of synchronizers
  - frequencies > 3 GHz
  - transistors have lower gain
  - severe layout parasitic capacitance

- Metastability characteristics:
  - both large-swing and small-swing signal behavior
  - possible to measure, but unable to use conventional simulation due to numerical stability and precision limits
  - possible to estimate from circuit equations, but non-trivial to analyze multi-stage synchronizers

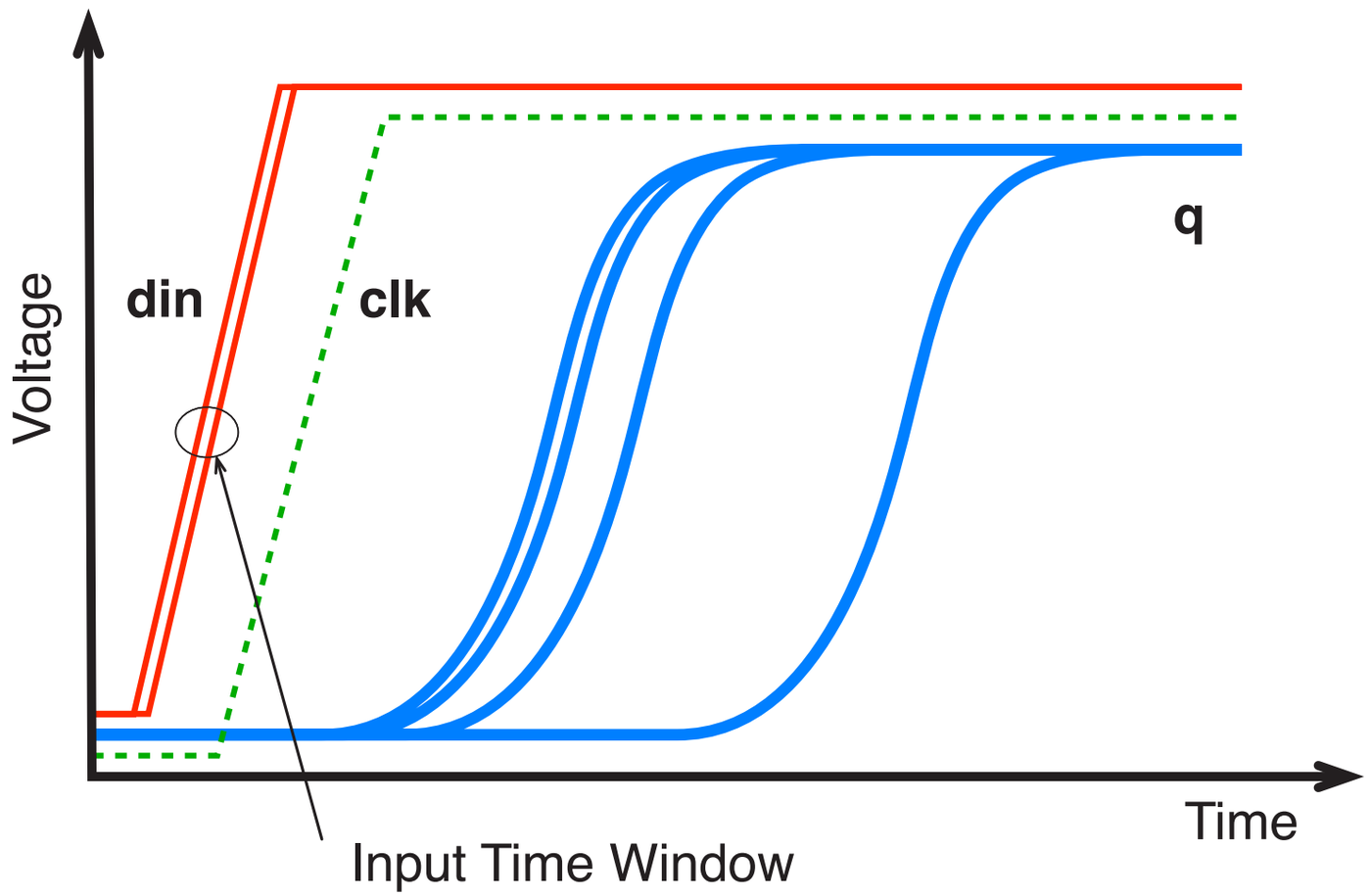
SIMMAT

A Metastability Analysis Tool

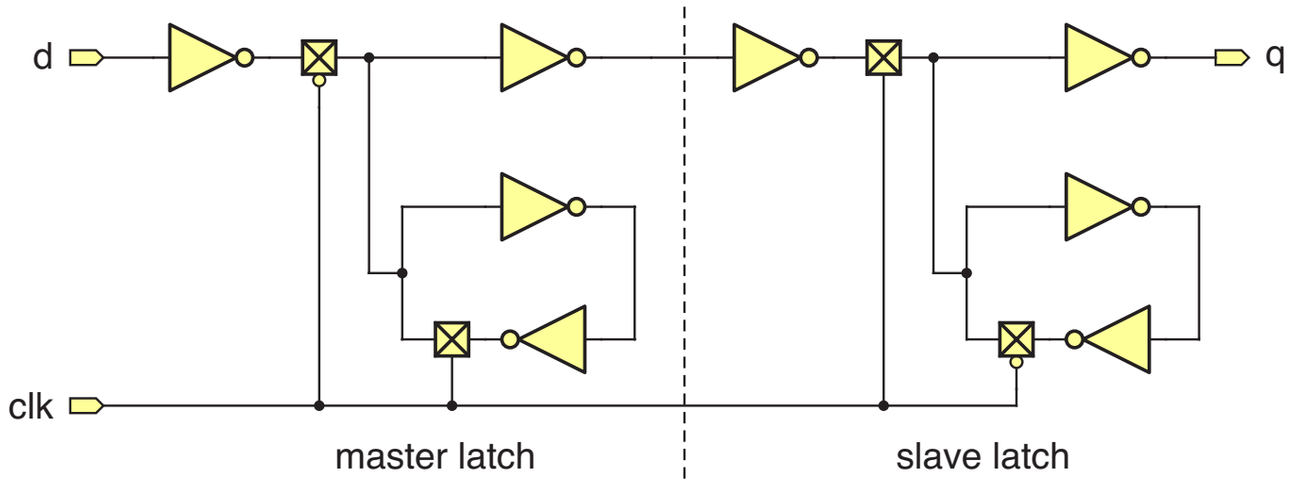
- Enables estimation of metastability characteristics during circuit design rather than after fabrication
- Built on top of conventional simulators, such as Hspice and SmartSpice
- Used for:
  - characterizing deep metastability behavior
  - comparing synchronizer circuits and layouts
  - evaluating effects of adding scan test circuits
  - exploring state machine failure resulting from prolonged metastability

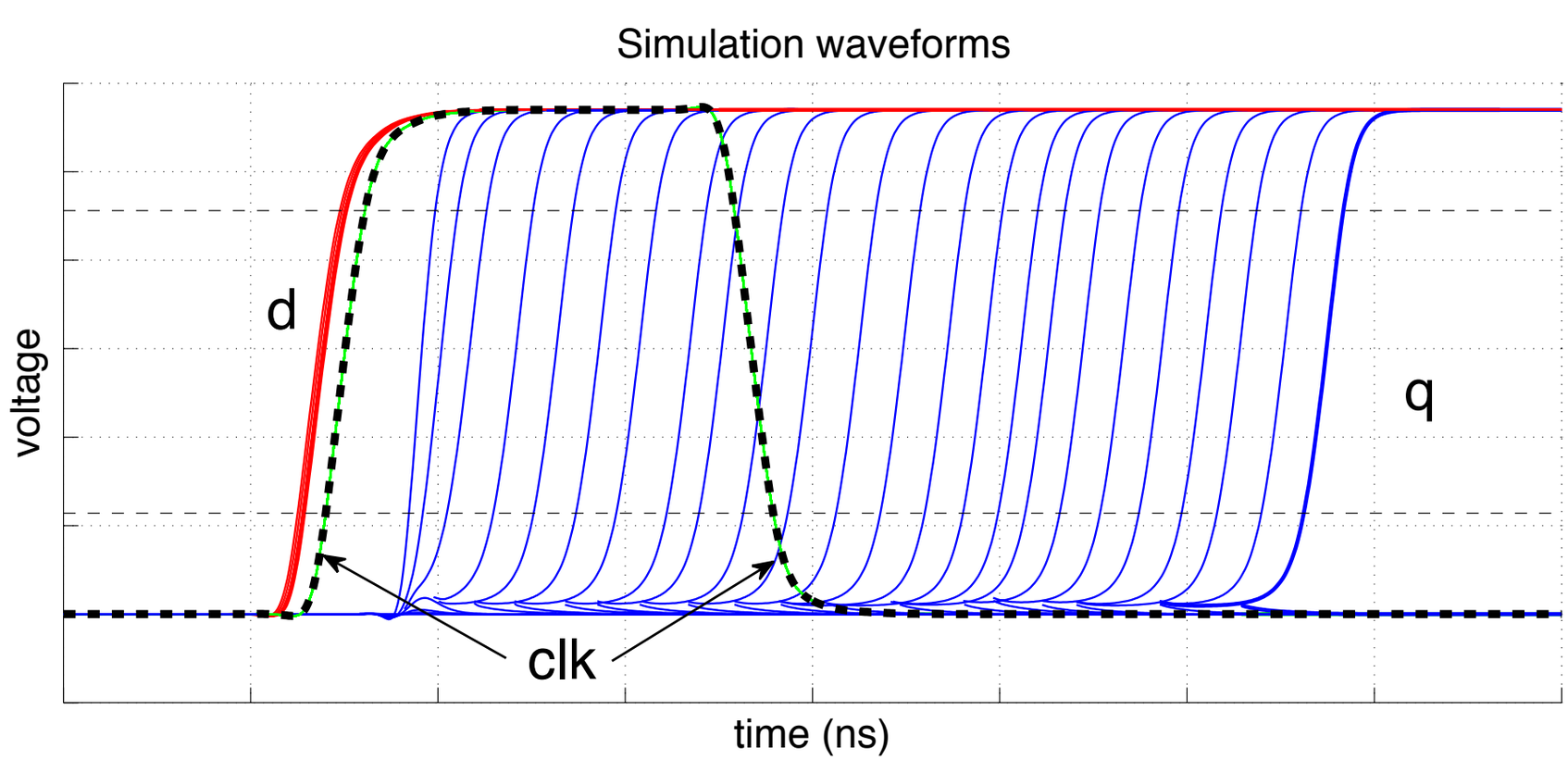
Increased Clk to Q Delay

Synchronizer circuit samples input data and decides if data are HI or LO. Occasionally the data are sampled when changing and the decision response is delayed – can cause circuit malfunction.



Synchronizer Analysis Waveforms





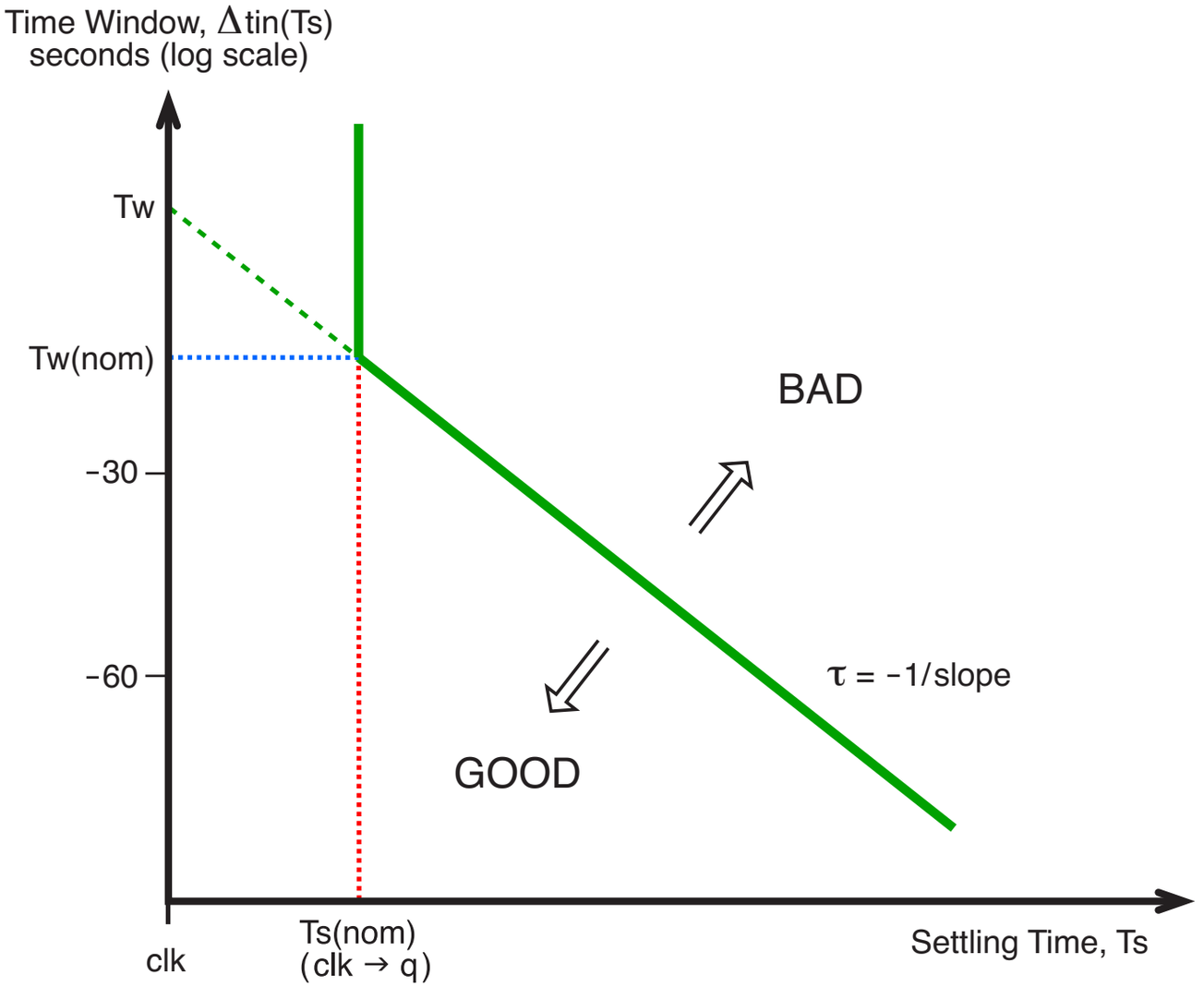
Synchronizer Characteristics

$$MTBF = \frac{\exp(Ts / \tau)}{Tw \times fc \times fd} = \frac{1}{\Delta tin(Ts) \times fc \times fd}$$

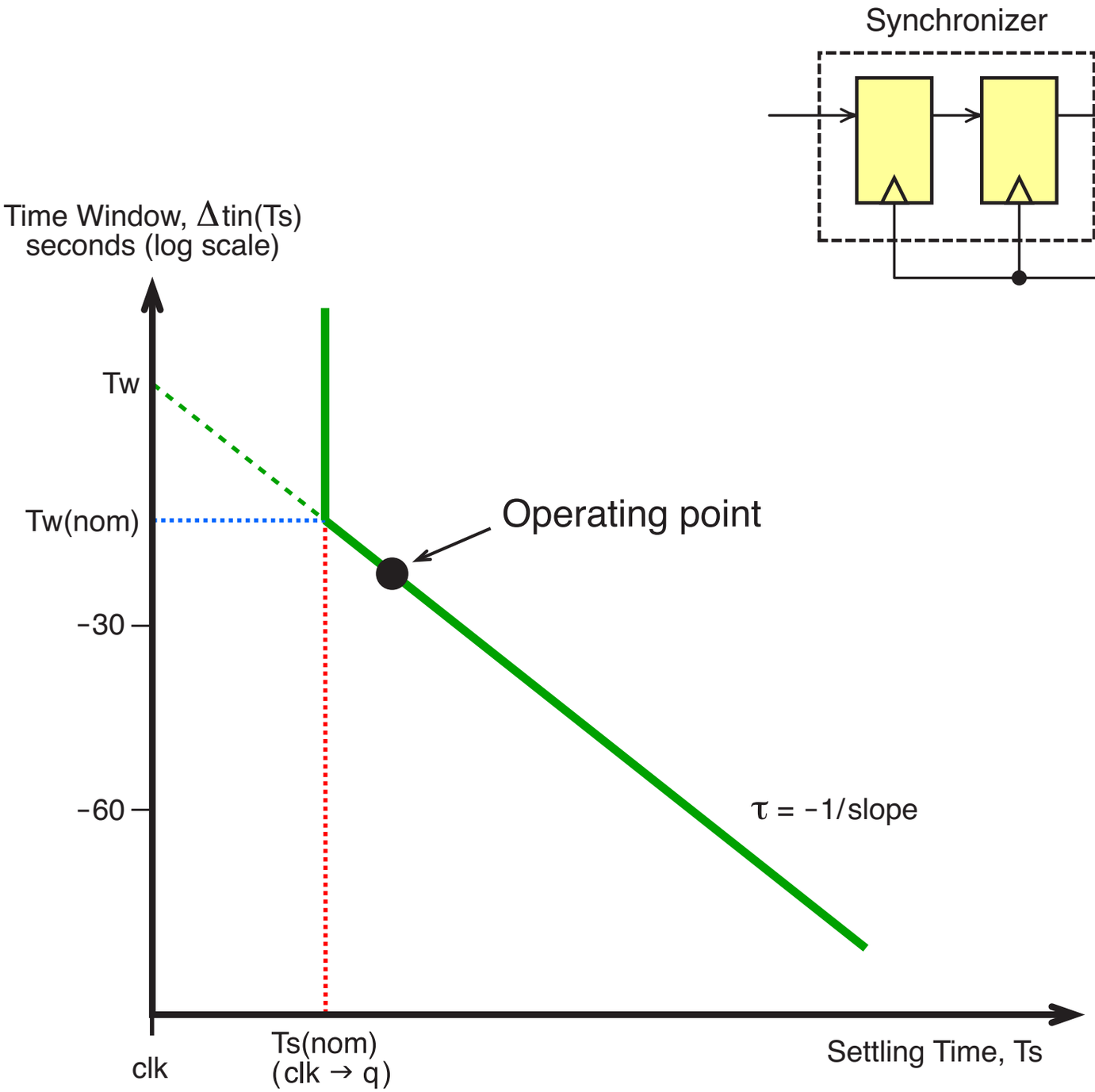
- Simulation analysis: Time Window size, $\Delta tin(Ts)$, for Settling Time values, Ts

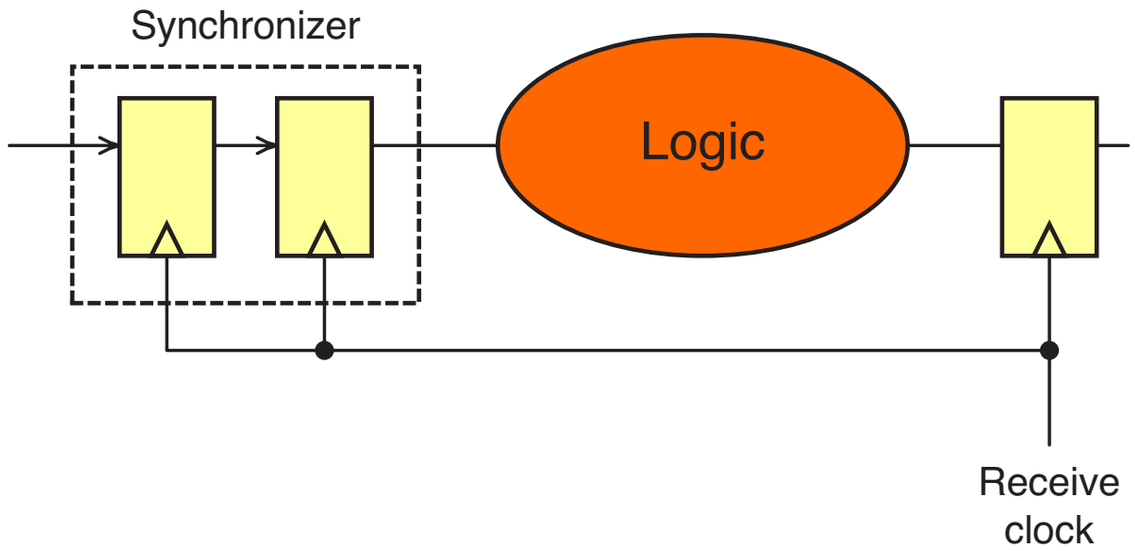
- Tw(nom) < setup + hold

- MTBF increases exponentially with Ts

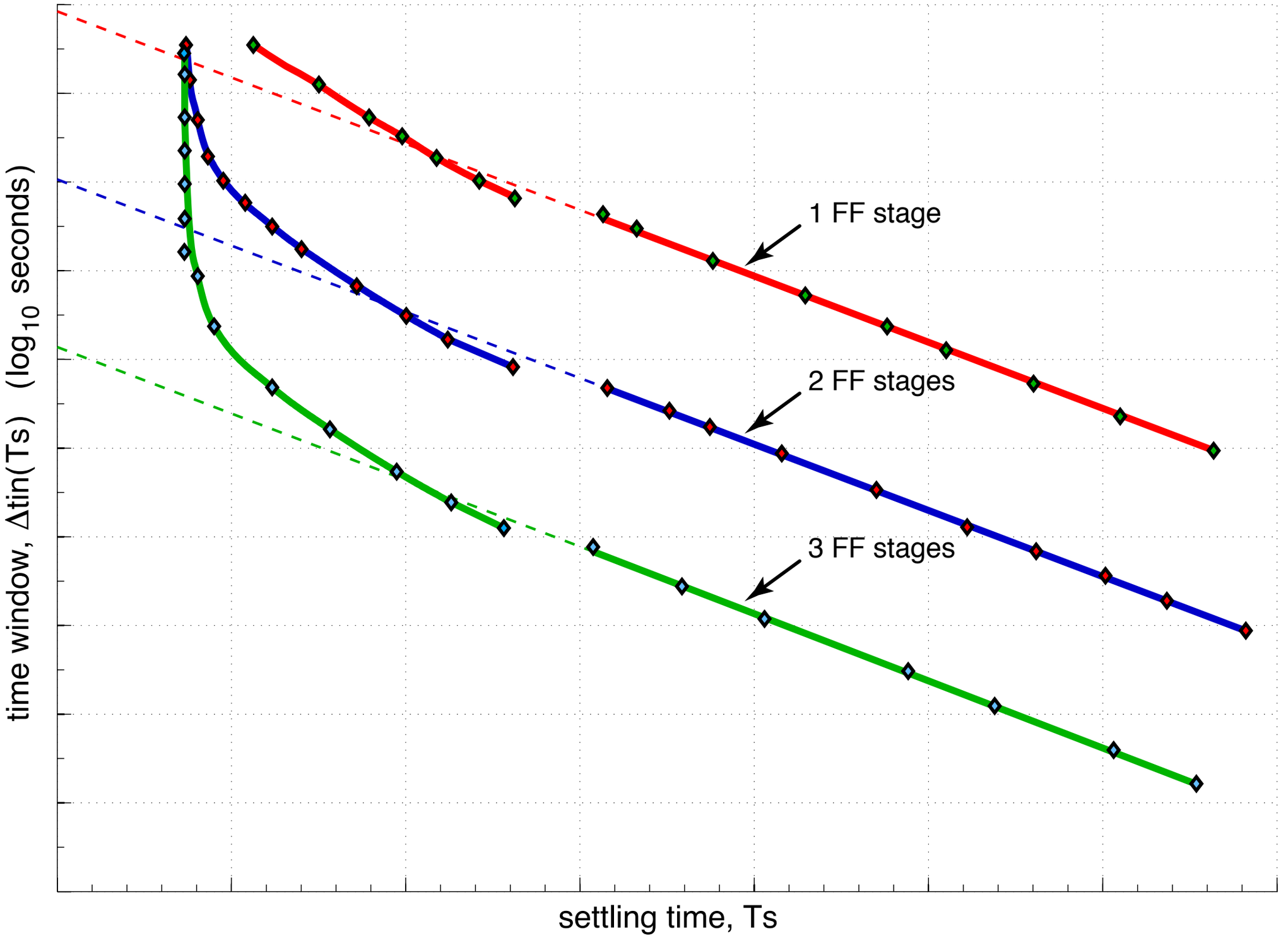


Operating Point





Metastability Analysis Results



Example MTBF Calculations:

A signal crossing into a 3 GHz clock domain from a 2 GHz clock domain, where the signal changes on average at 0.25 * 2 GHz

fc = 3 GHz, fd = 0.25 * 2 GHz, at Ts = clock-to-q delay + slack time:

- 1 FF stage: Δtin(Ts) = 10**-17 seconds

  MTBF = 1 / ((10^(-17 + 18)) * 3 * 0.25 * 2) = 60 msec

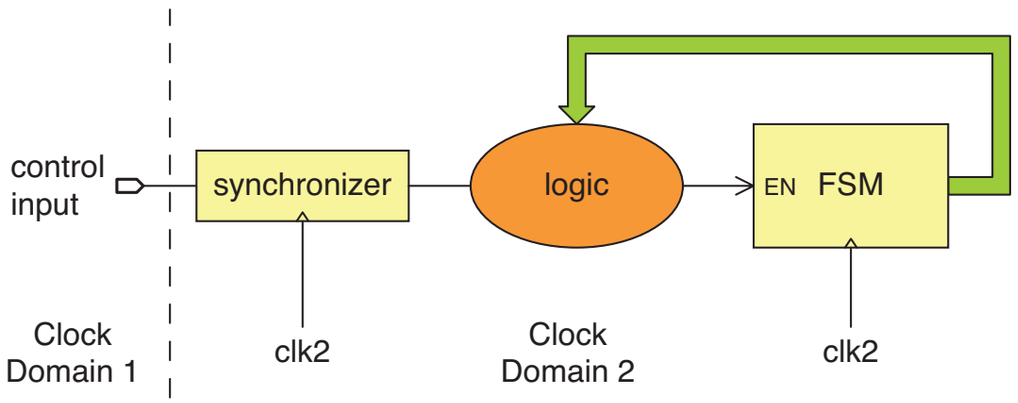
- 2 FF stages: Δtin(Ts) = 10**-26 seconds

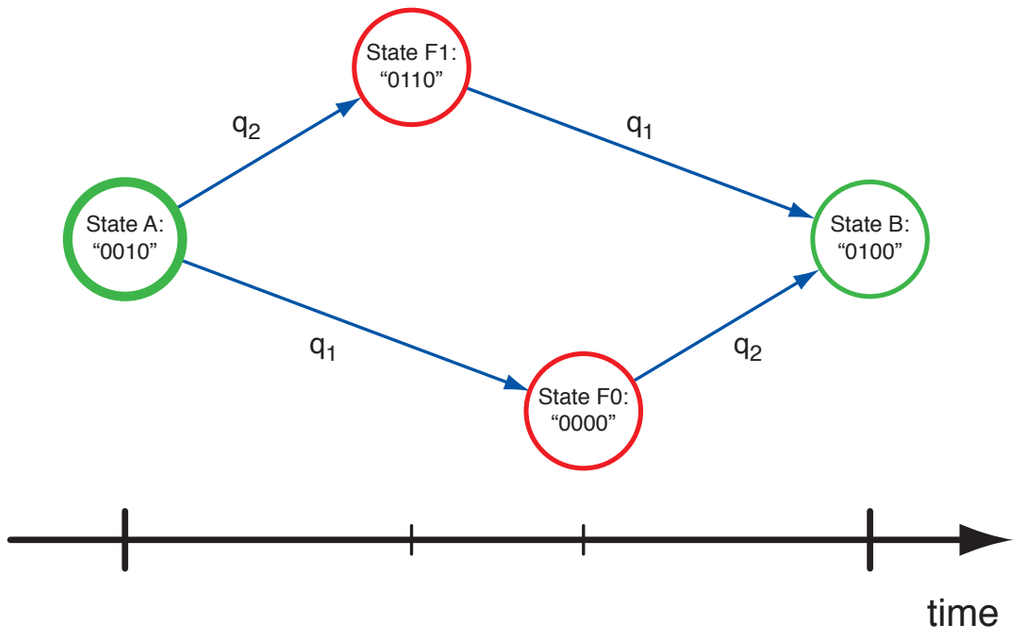
  MTBF = 1 / ((10^(-26 + 18)) * 3 * 0.25 * 2) = 2 years

- 3 FF stages: Δtin(Ts) = 10**-37 seconds

  MTBF = 1 / ((10^(-35 + 18)) * 3 * 0.25 * 2) = 2e+9 years

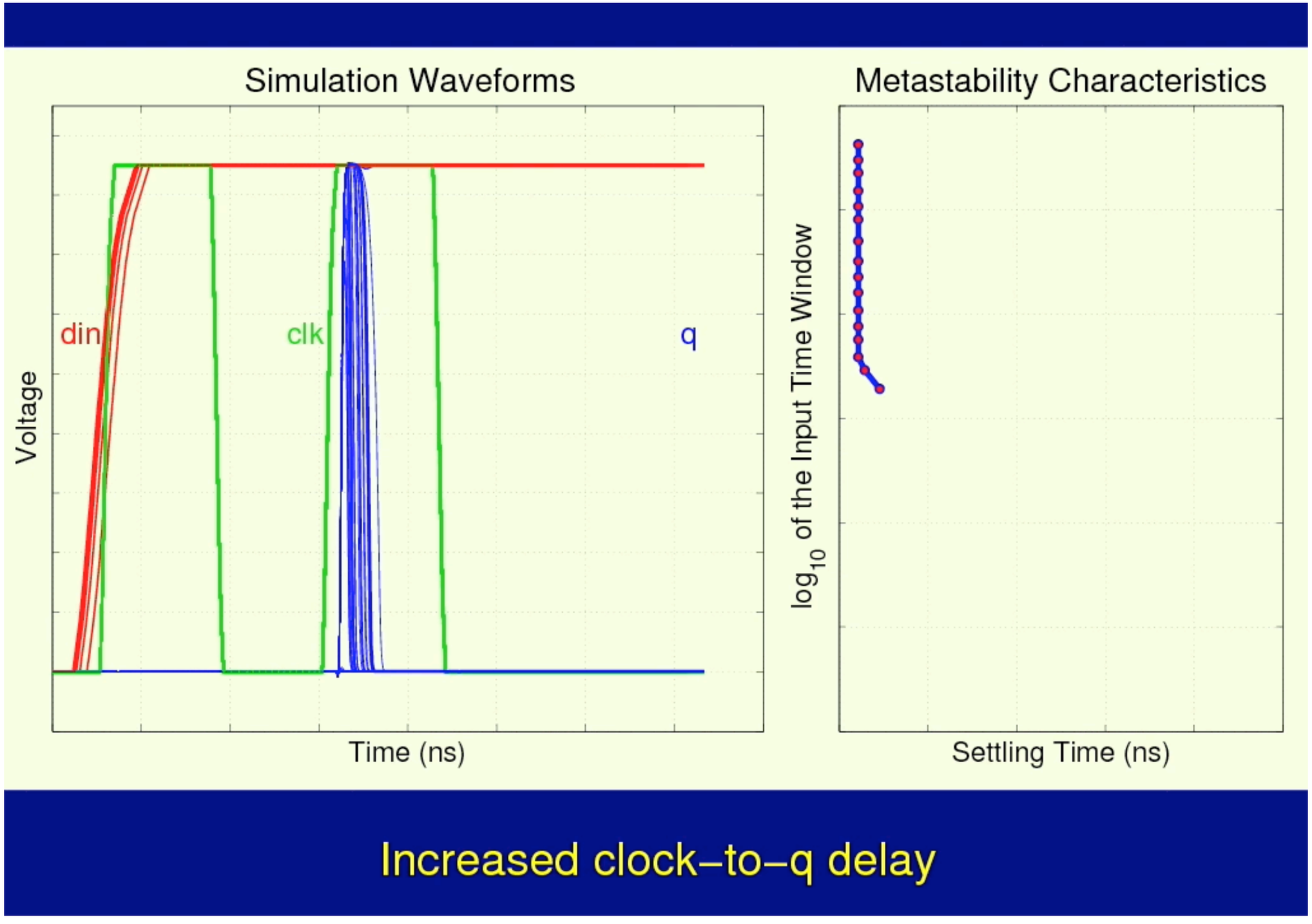
State Machine Failure





- State change from “State A” to “State B” enabled by control signal output from a synchronizer
- State change involves multiple bit transitions
- Delayed synchronizer response can produce an incomplete state change, ending in failure states “State F1” or “State F2”
- Can use SIMMAT to analyze the failure probability

Video Animation



Increased clock–to–q delay

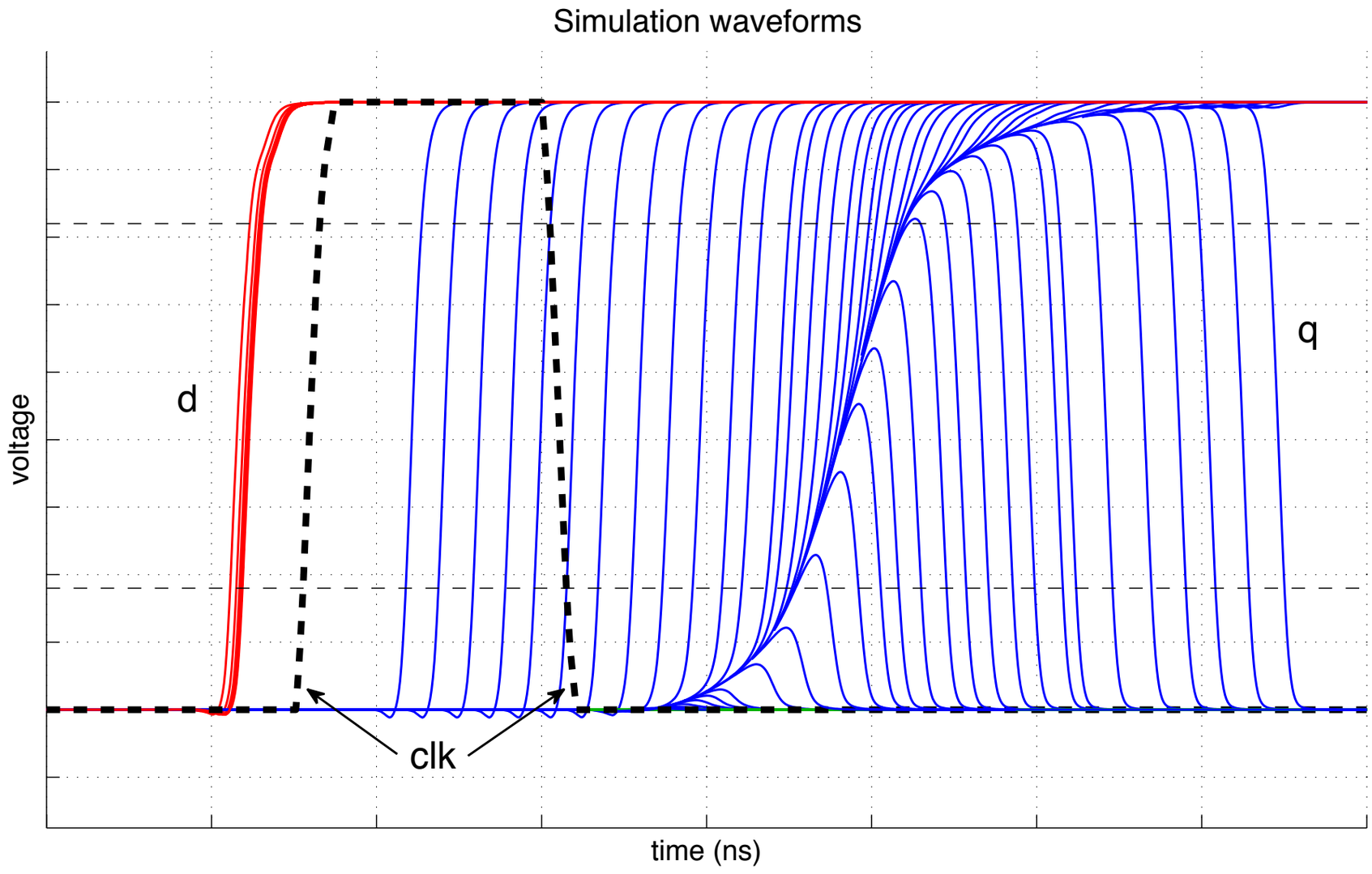
Conclusion

SIMMAT:

- Enables analysis of multi-stage synchronizers in deep metastability
- Characterizes synchronizer circuits ➜ MTBF
- Facilitates design of new circuits
- Explores bi-modal circuit behavior

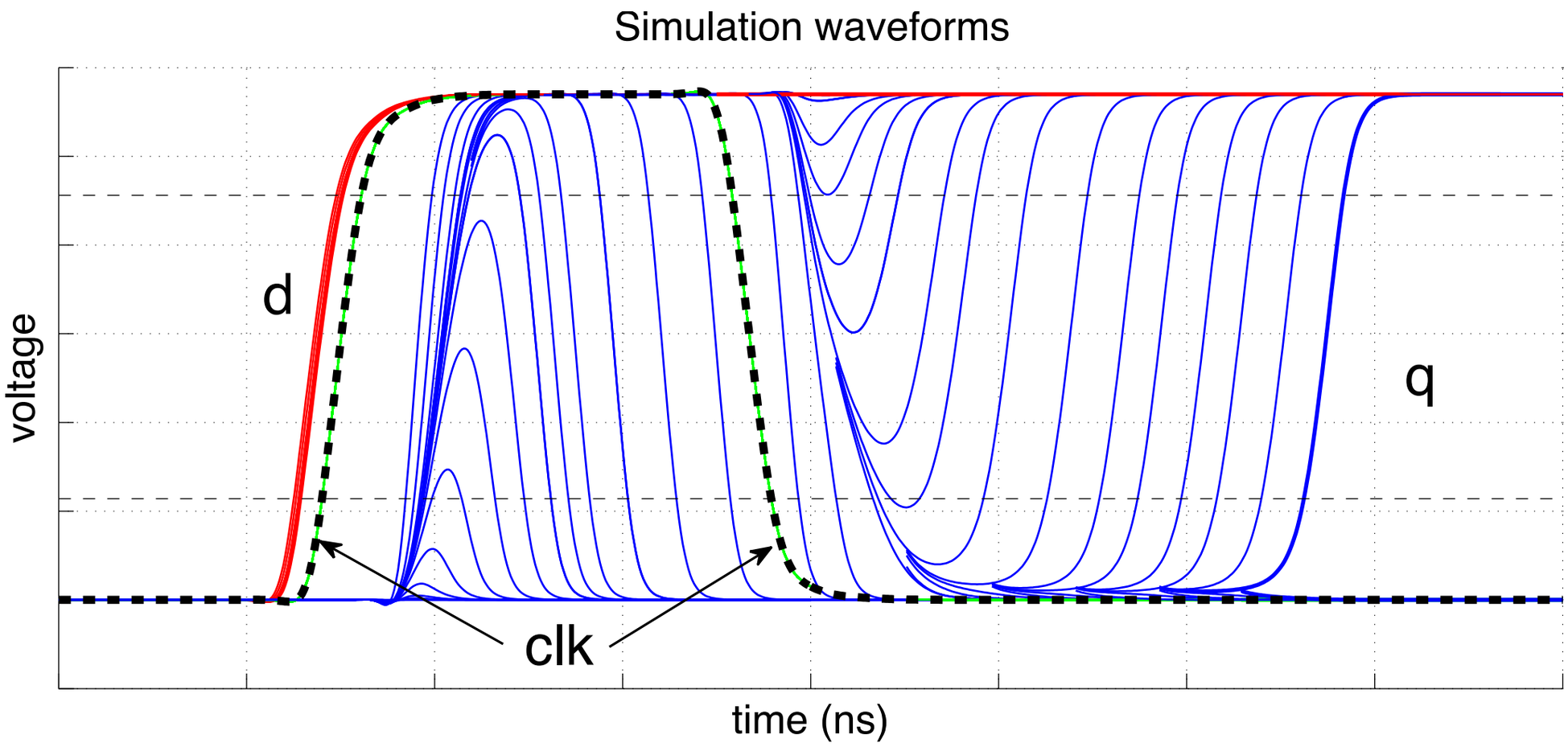
Extra Slides

Long Time-constant Output



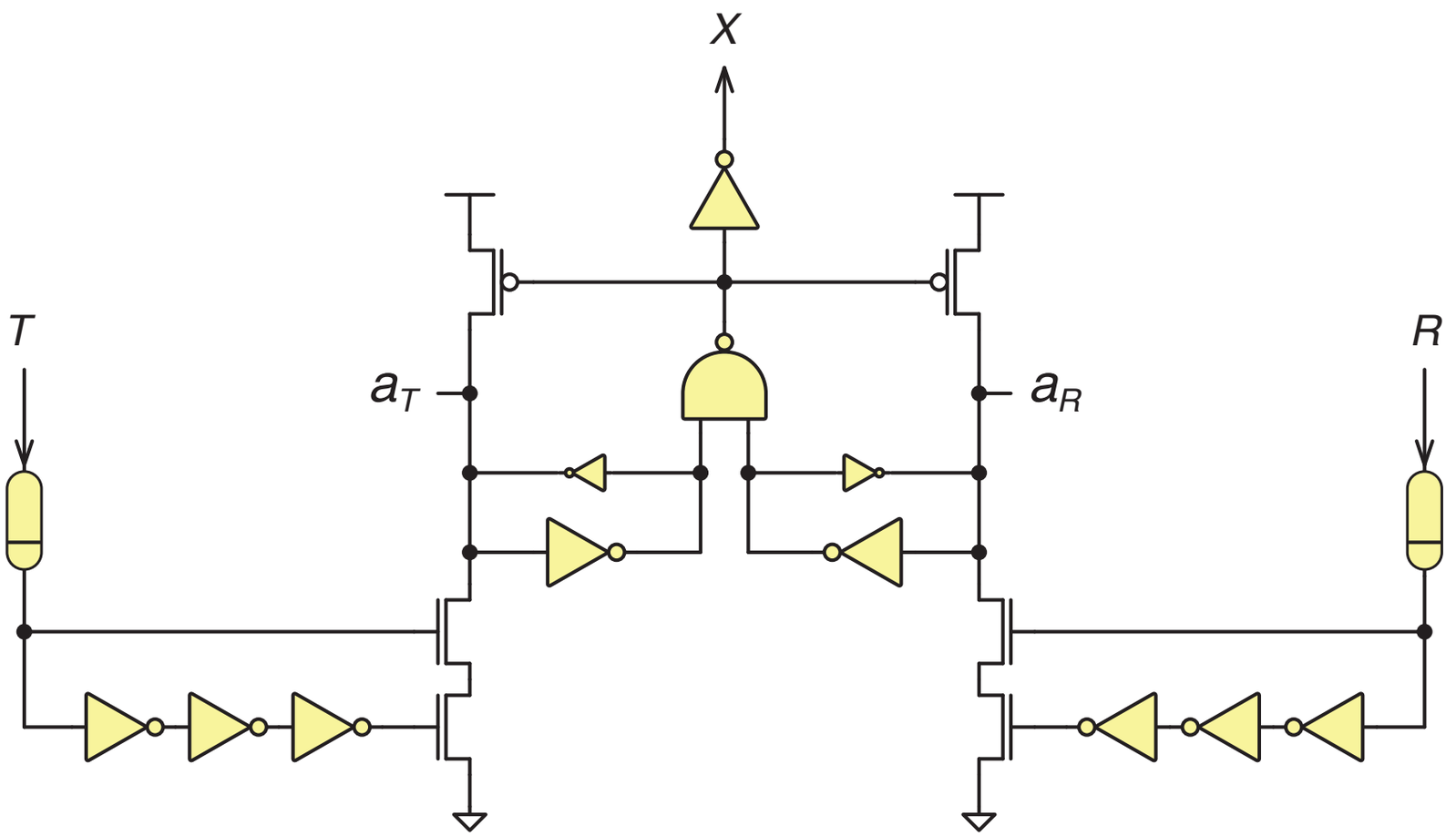
Output amplifier has switching voltage very close to metastable voltage of slave latch

Multiple Output Transitions



Master and slave latches have slightly different metastable voltages while the switching voltage of the output amplifier lies between these two voltages

Metastability During Initialization



Clock-phase generator for source-synchronous communication

A self-resetting gate that during initialization can exhibit metastability that persists for multiple clock cycles