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Estimating MTBF of Multi-Stage Synchronizers

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Synchronizers Essential in Multi-Synchronous SoCs

- Low-skew, global clock trees problematic
- Survey of proposed SoC design starts*
  - 32% contain > 50 clock domains
  - 12% contain > 100 clock domains
- Each CDC requires reliable synchronization

* Survey by Graham Bell, Director of Marketing, Real Intent, Inc. See: http://www10.edacafe.com/blogs/realintent/2012/09/27/dac-survey-on-cdc-bugs-x-propagation-constraints/

Old Rules of Thumb* Unreliable

- Problematic because of increases in
  - Clock speeds
  - Data rates
  - Number of CDCs
  - Semiconductor process variability
  - Tau (low power $\rightarrow V_m \sim V_t$)
- FO4 no longer predicts tau
- Negative temperature coefficient of V_t

* Two FFs in cascade are almost always enough, but when you are worried, use three.

Determining Synchronizer MTBF

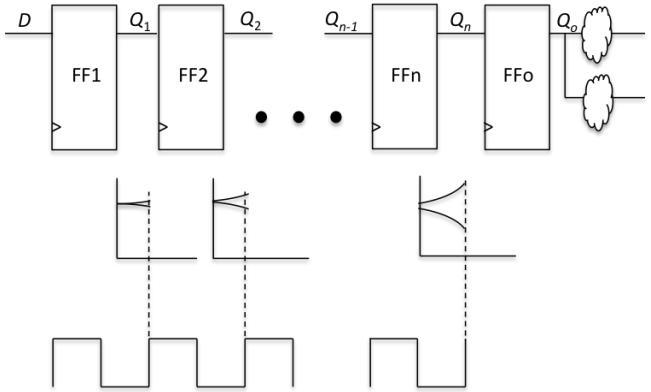
- Intrinsic parameters - vary with PVTA
  - Settling time-constant τ_{eff}
  - Number of stages n
  - Aperture width $T_W(n)$
- Extrinsic parameters - vary with application
  - Clock rate f_C
  - Data transition rate f_D
  - Duty cycle α

Determining Synchronizer Parameters

- Physical measurements $\rightarrow$ protracted testing
  - Testing at PVT corners – impractical number of runs
  - Testing multi-stage synchronizers – interminable
- Circuit simulation $\rightarrow$ automated, pre-fab testing
  - Synchronizer standard-cell designer specifies:
    - Intrinsic parameters: τ_{eff}, n, $T_W(n)$
  - Synchronizer standard-cell integrator specifies:
    - Extrinsic parameters: f_C, f_D, α
  - MTBF formula for a multi-stage synchronizer needed

Some Multi-Stage Formulas

Over the years, many ways to estimate MTBF in multi-stage synchronizers have been presented in the literature. Here are three common forms:



- Kinnement, Altera and others: MTBF(n) is proportional to waiting *n* times as long. (2007)
- Kleeman, et al: routing delays and setup time reduce resolving time of each stage. (1987)
- Gabara, et. al: master and slave latches have independent T_W. (1992)

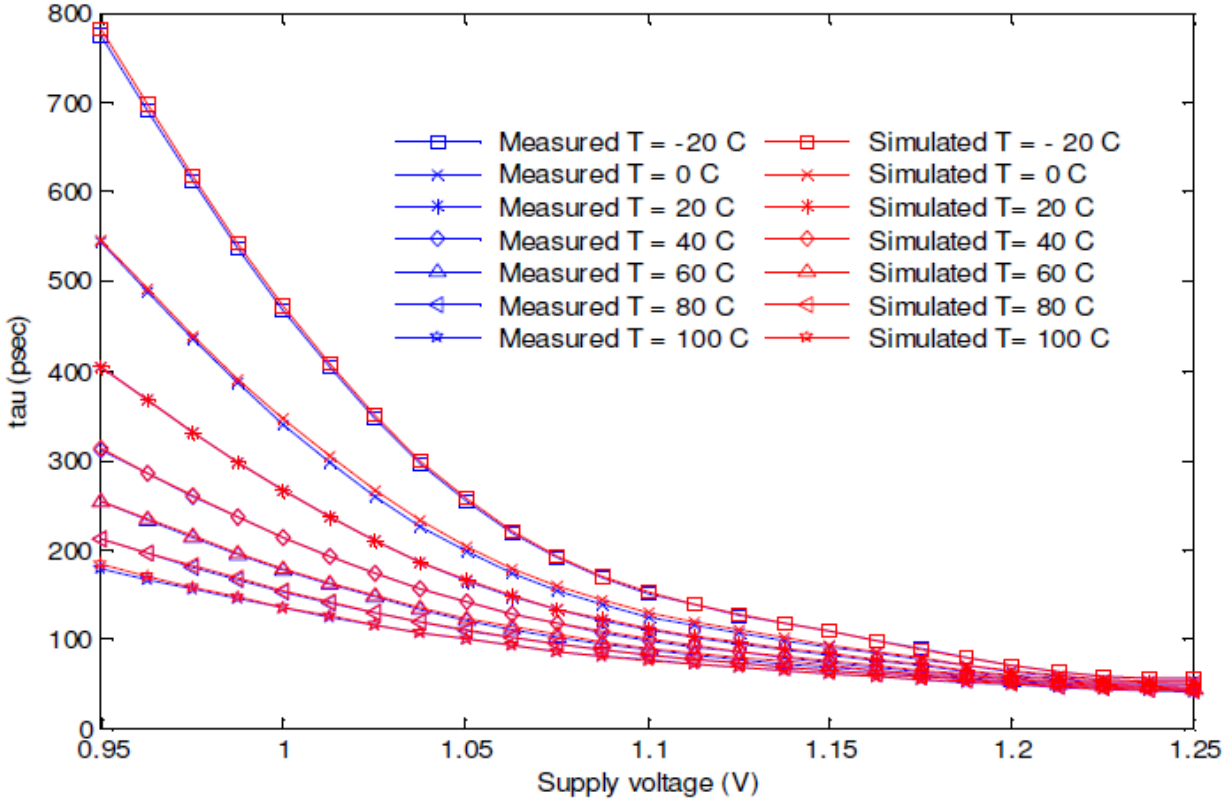
$$MTBF_{Kinniment}(n) = \frac{exp[nT_C/\tau]}{T_W f_D f_C}$$

$$MTBF_{Kleeman}(n) = \frac{exp[(nT_C - nt_p)/\tau]}{T_W f_D f_C}$$

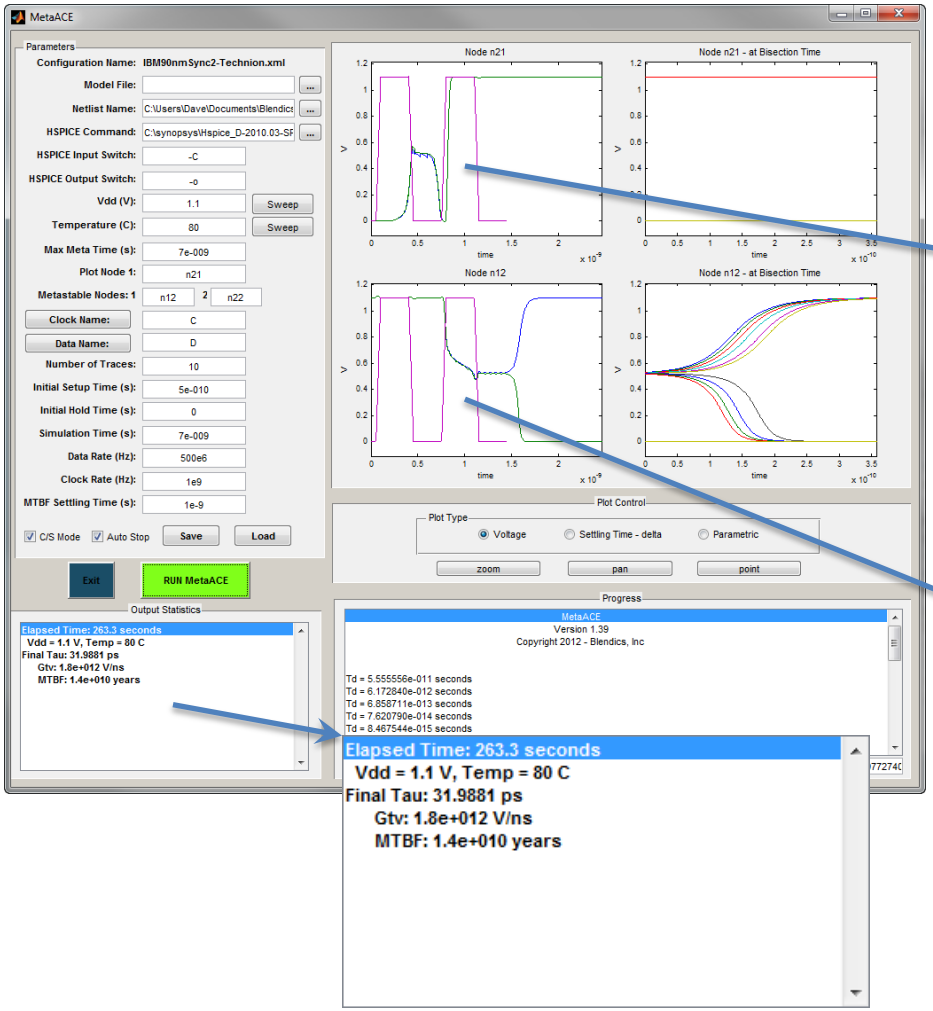
$$MTBF_{Gabara}(n) = \tau \frac{exp[(nT_C - 2nt_S^S)/\tau]}{T_W^2 f_D f_C}$$

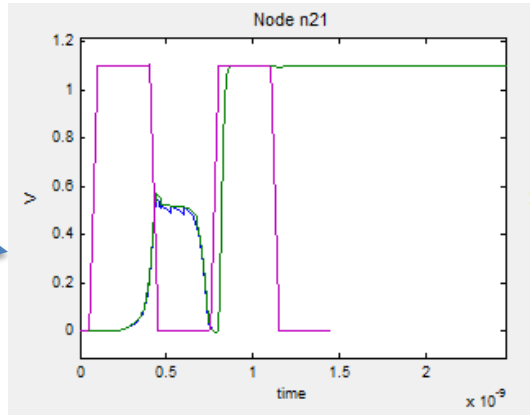
Simulation vs. Measurement

- Simulating with *MetaACE*, we compared a latch τ with measurements on a 65 nm, low-power circuit ($\tau \pm 5\%$).

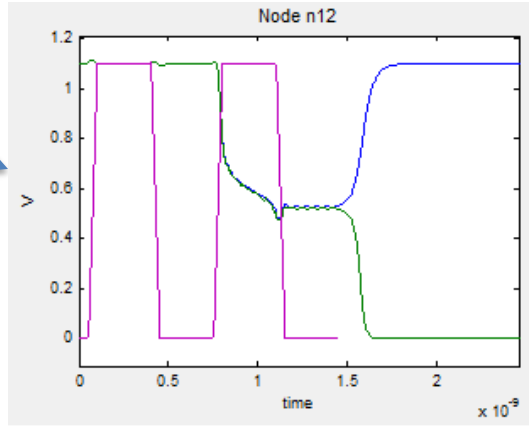


Some *MetaACE* results



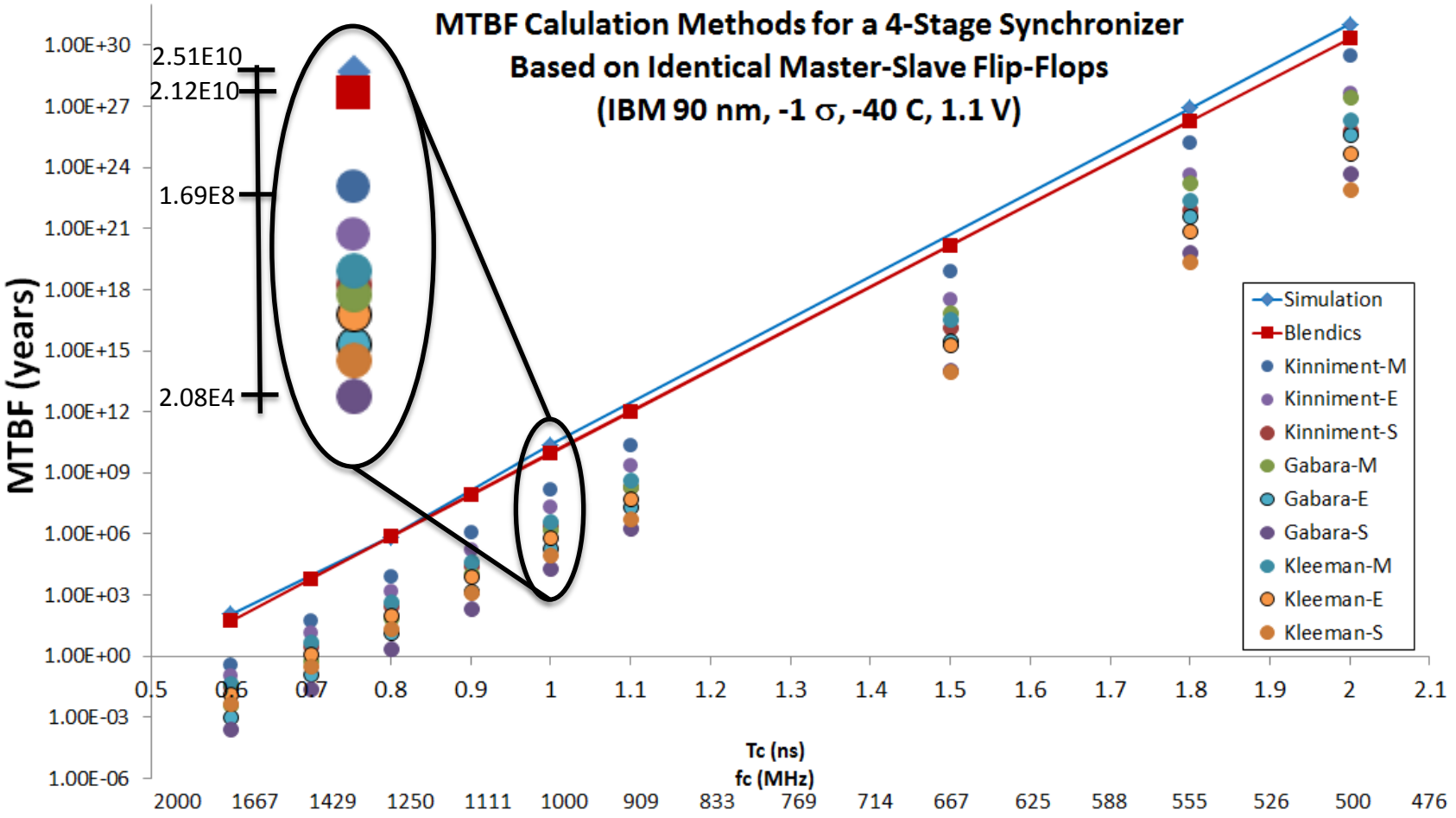


Output of First Flip-Flop



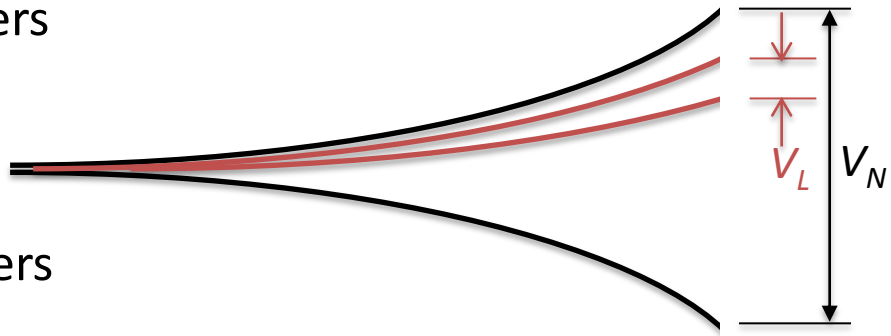
Output of Second Flip-Flop

Comparison of MTBF Results



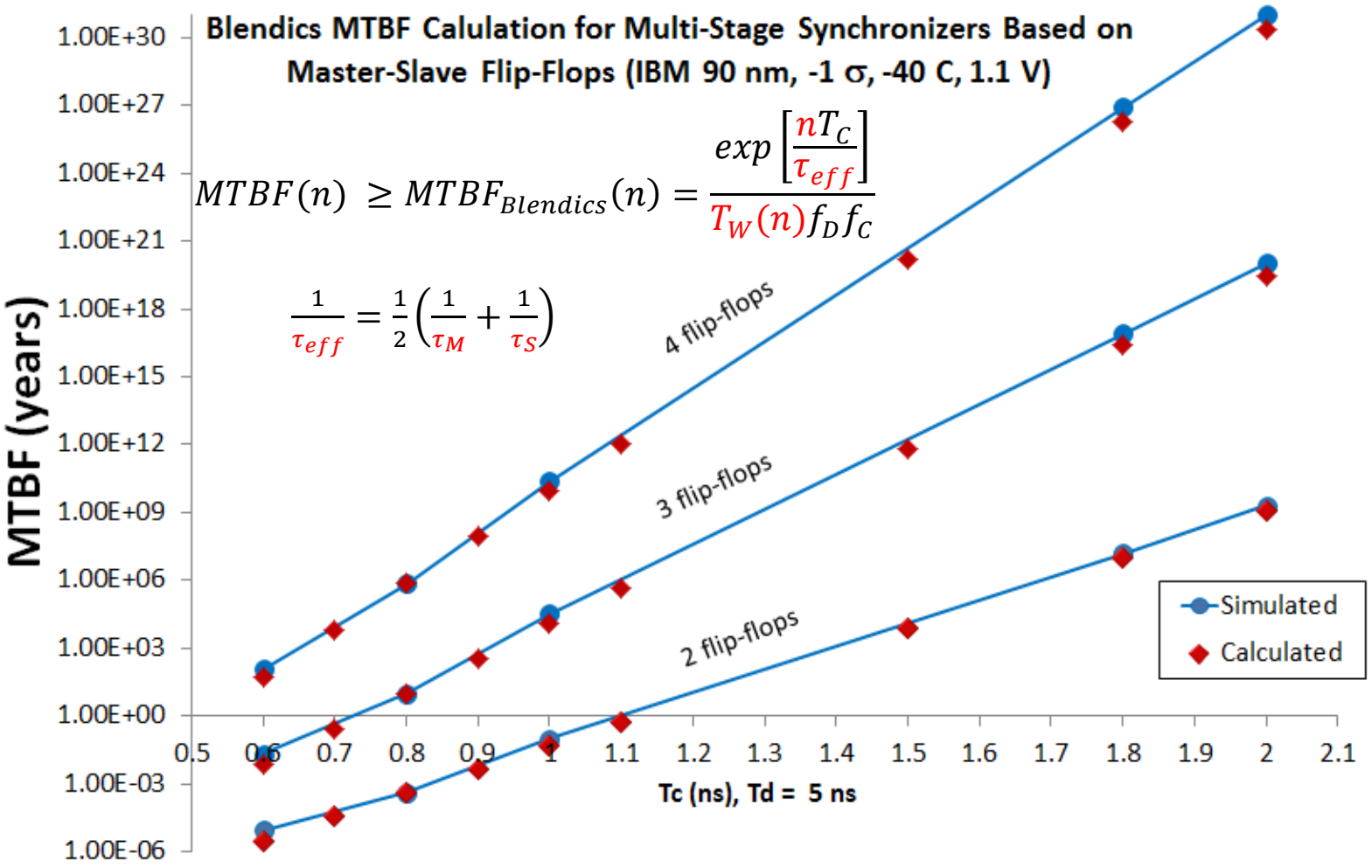
Published Formulas Conservative

- Existing formulas treat inter-stage coupling conservatively
- Voltage traces leaving metastability
  - V_N is voltage range that covers invalid, next-stage outputs.
  - V_L is voltage range that covers invalid, last-stage outputs.



- For multi-stage synchronizers $V_L << V_N$ and as a result MTBF based on V_L can much greater than that based on V_N
- Therefore must simulate entire synchronizer

Estimation of MTBF by Formula



Predicting Synchronizer MTBF Important

- More multi-synchronous SoC designs
- Low-voltage circuits increase τ
- Low-temperature operation increases τ
- Semiconductor variability increases failure risk
- Failures hard to recognize in silicon
  - Must have accurate MTBF before fab
  - MTBF can be calculated from τ_{eff} , n and $T_w(n)$

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