Leveraging the geometric properties of on-chip transmission line structures to improve interconnect performance: A case study in 65nm

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***Abstract*— Implementation of low energy, low latency transmission line interconnects on a network-on-chip presents the circuit designer with a variety of structural design choices. This work presents a study of the comparative effects of changing the wire geometries on the latency, energy dissipated, area, and noise properties of the transmission lines. These results will aid the engineer in the design and performance analysis of the global interconnect and foster a quantitative understanding of the wave signaling properties in the RLC regime.**

Energy dissipation in wires has become a primary bottleneck for the continued scaling of future interconnect networks. Packet switching on high radix network topologies exacerbates this problem due to the energy and latency overhead contributed by switches and routers. Alternative network fabrics utilizing low latency, low energy buses have shown promise in circumventing this problem [1]. Transmission lines (TL) are possibly the most suitable building blocks for bus-based topologies since they provide fast, low energy long distance communication using present generation CMOS devices and techniques. Reliable on-chip implementation of TL interconnects requires substantial analysis and careful design, often with the help of complex full-wave field solvers. Characterization of transmission lines is a well studied subject [2] [3] [4]; however, a direct relation between the physical and geometric properties of a TL link design and its effectiveness as a communication medium is not available. This work aims at providing an insight into the various trade-offs between the performance of global RLC wires and their geometric properties. The case study presented here is intended to serve as a guide for link designers to better understand the available design choices supplemented with numerical data.

RC representations of long wires are rendered inaccurate due to high frequency inductance effects. Electromagnetic field solvers are required for analyzing the behavior of transmission lines in order to include second order effects such as substrate coupling. Since accuracy trumps solution time in this study, a 3D full wave solver is employed for the analyses [5]. Scattering (S) parameters are extracted from the TL geometries for a frequency range of 100 MHz to 100 GHz and written to a Touchstone file for over 50 different transmission line structures. Transient analyses are performed on these extracted values in Synopsys HSPICE using CMOS drivers and loads. The back end of the line (BEOL) arrangement from the Global Foundries 65nm LPE process, complete with a hierarchical dielectric structure, low resistivity substrate and dense lower metal layers, is used as the guide to set up the simulation environment. Tab. I summarizes the parameters corresponding to this BEOL stack. The coplanar and microstrip transmission line configurations as shown in Fig. 1 are studied. The design parameters in this study are the widths of the signal and ground paths, and the spacing between them. All evaluations are made for 5mm links, which is the typical length for medium to long distance communication on a modern chip. Transient simulations are performed at frequencies of 5 GHz, 10 GHz, 15 GHz, and 20 GHz.

TABLE I: BEOL stack information

Parameter	Values
Metal layers	6 (4 normal + 2 thick)
Top metal thickness	1 μm
Permittivity lower dielectric	3.0
Permittivity higher dielectric	3.6

Energy consumption in a transmission line link is reduced due to the absence of repeaters. They are eliminated by the wave signaling nature of data propagation. Our results show that increasing the frequency of data transfer does not increase the average power dissipated in the link; therefore operating at higher speeds results in lower energy per transferred datum. The simulations also show that changing the signal wire width has very little effect on the energy dissipated in the link as seen in Fig. 2a. Therefore, the width of the signal line can be increased to boost the signal integrity or decreased for area considerations without having to worry about the energy budget. Fig. 2d shows that wider ground wires bring better coupling between the signal and return paths and therefore marginally reduce the energy dissipation. Also to be noted is the fact that the microstrip configuration of transmission lines demonstrates better energy performance as compared to the coplanar configuration.

A major win in the argument for adoption of TLs as global interconnects is the near speed-of-light velocity of signal propagation. The propagation delay depends on the effective permittivity of the dielectric surrounding the wires, which relates to the arrangement of the wires and therefore differs in the cases of coplanar and microstrip topologies. The effective permittivity changes significantly for microstrip lines when the signal width is varied, therefore changing the latency. Microstrip lines have nearly identical latencies for all signal width values under consideration as shown in Fig. 2b. Conversely, Fig. 2e shows that when the ground wire width changes, the latency of both configurations only decreases slightly. Simulations show that coplanar lines outperform microstrip lines in the matter of link latency.

One of the fundamental issues with implementing transmission lines over low resistivity silicon substrates is their

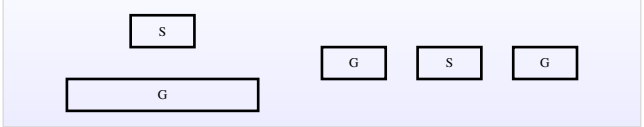
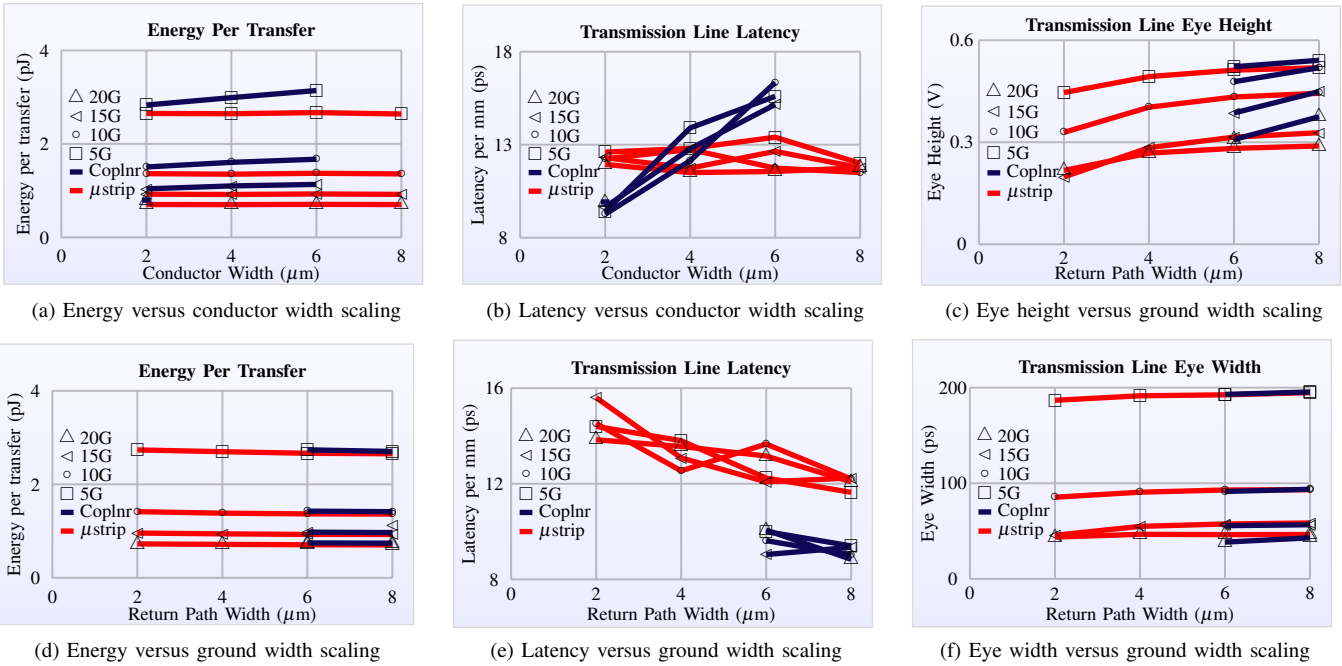


Fig. 1: Cross section of microstrip and coplanar waveguides



(a) Energy versus conductor width scaling

(b) Latency versus conductor width scaling

(c) Eye height versus ground width scaling

(d) Energy versus ground width scaling

(e) Latency versus ground width scaling

(f) Eye width versus ground width scaling

Fig. 2: Energy, latency, and eye height and width as conductor and ground widths are scaled

sensitivity to noise. In this work, eye diagram analysis is used to evaluate the channel noise characteristics. The eye height is the measure of the amplitude fidelity of the channel. On the other hand, the eye width captures the effect of frequency dependent losses on the rise and fall times of the transmitted signal. Simulations show that the eye height progressively decreases as bit rate increases. Dielectric losses become dominant close to 20 GHz and result in the closing of the eye. Eye height values remain fairly constant with variations in conductor width. Changing the width of the return path has a remarkable effect on the eye height. For example, a 65% gain in eye height is observed when the ground wire width of a microstrip line is increased from 2 μm to 8 μm at 15 GHz, as seen in Fig. 2c. Microstrips perform decidedly better than coplanar wires in the timing fidelity metric. They exhibit a wider eye as well as more robustness to changes in conductor width as compared to coplanar lines. Wider return paths provide better coupling and consequently improve the eye width of the received signal, as observed in Fig. 2f.

In addition to requiring thick, top level metal layers for reliable implementation, TL wires have larger pitches when compared against minimum pitch RC wires. This is due to the minimum constraints imposed on signal and return path dimensions along with spacing requirements to ensure correct transmission line behavior [6]. Coplanar lines have return paths on either side of the signal path on the same metal layer which results in wider pitches. Such a configuration provides excellent noise rejection from aggressor lines on the same layer, but suffer from crosstalk induced by wire currents on vertically adjacent layers and the substrate. Conversely, microstrip lines have return paths on a separate metal layer than the signal paths. The pitch of this configuration depends on the return path width. Smaller pitch microstrip lines are more susceptible to crosstalk from neighboring wires on the same metal layer. Also, this arrangement necessitates the use of two consecutive top metal layers running in the same direction on the chip, which is a high price to pay for global interconnects.

The purpose of this work is to aid the designer in making suitable choices from the available design space to achieve link performance goals. If energy is the primary concern, a microstrip line running at a high data rate is the optimal choice. To decrease the propagation delay value, the correct choice is to employ coplanar wires with wider return paths. Wide return paths also provide better noise resistance to the TL medium. If there are a number of aggressor lines on the same metal layer, a coplanar wire is more suitable; whereas microstrips provide better resistance from substrate coupled noise as well noise from dense, lower layer wires. These design guidelines enable the network-on-chip architect to make informed choices in order to maximize the performance of the low latency, low energy transmission line channel.

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