



Editorial

Selected papers from the 16th IEEE International Symposium on Asynchronous Circuits and Systems

Asynchronous designs employ handshaking to perform communication and data transfer between elements in a system. This method was employed in computer architecture as early as the 1950's. Much has changed since those early days. Rather than design with vacuum tubes and discreet devices, current technology enables designs that can have billions of transistors with 32 nm feature sizes. Asynchronous design technology has likewise advanced. The International Symposium on Asynchronous Circuits and Systems (ASYNC) is the premier forum covering recent technological advances in this area of research. This annual conference brings together researchers and industry experts from around the world to discuss a broad range of topics covering all aspects of asynchronous design and related emerging technologies.

Research and interest in this broad and diverse field has grown substantially since the conference series was first started in 1994.

This includes traditional core topics of design, synthesis and test; asynchronous applications in system-level integration and emerging computing technologies such as hybrid clocked designs that employ handshaking to achieve latency insensitivity; and novel methods of addressing process variability and substantially reducing power. This Special Issue contains three papers that cover a broad spectrum of research and application of asynchronous technology to today's design problems.

The increasing contemporary interest and application of this technology is due to several factors. Firstly, scaling continues unabated resulting in exponential increase in the number of components on a chip. This in turn makes it difficult to design a global clocking network that can, in an energy efficient manner, globally synchronize all components on a chip. Secondly, a shorter time-to-market and the increased design complexities have resulted in the re-use of design blocks. Each of these blocks are designed for, and will optimally function at, different frequencies. Such a design methodology is common in the System on Chip domain today where tens of frequencies may exist on a chip. Thirdly, as technology features continue to scale down, the effects of process

and environmental parametric variations call for variation-tolerant circuit designs. Finally, power has emerged as one of the primary design challenges facing the semiconductor industry today. One of the few approaches that enable a substantial reduction in power is asynchronous design technology. The three papers chosen for this Special Issue do a good job of covering key aspects of this diverse technology.

The first paper by Casu applies asynchronous methodologies to clocked design in such a way that it allows a clocked design flow to adopt many of the advantageous aspects of asynchronous design. Handshaking is added to the clocked data paths, which creates a latency-insensitive protocol. This paper discusses an optimisation of the clocked handshaking control components by allowing retiming and token cages that employ early evaluation. These transformations increase the throughput of latency insensitive systems.

The second paper, by Toms and Edwards, addresses logic synthesis for datapath circuits that employ delay-insensitive m-of-n codes in order to increase robustness to delay variation. The problem of decomposing and mapping large function blocks expressed as m-of-n codes to cell libraries is known to be extremely hard because it requires indication of the cells in the intermediate layers of logic. This problem is elegantly addressed in this work by decomposing input m-of-n encodings into smaller unordered codes. Two efficient algorithms for determining such unordered codes are presented and applied to a number of benchmark circuits.

The results presented in the third paper, by Akgun, Rodrigues, and Sparsø, lower circuit power while substantially improving performance. This work operates the circuits in the sub-threshold regime. These circuits achieve energy minimal computations for their design, and the flow was validated on a chip fabricated in a 65 nm process. Current sensors are used for completion detection to achieve higher performance, shown at over 50% in a fabricated chip, with a power reduction of over 15%.

We hope that you will find this Special Issue informative, and that it will generate more interest by researchers and

industry practitioners in creating asynchronous techniques, tools, and circuit designs. We would also like to take this opportunity to thank the authors, the reviewers, and the editorial staff at the IET for their help in compiling this Special Issue.

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Kenneth S. Stevens is an Associate Professor of Electrical and Computer Engineering at the University of Utah. He holds a B.A. degree in Biology, as well as B.S., M.S., and Ph.D. degrees in Computer Science from the University of Utah and the University of Calgary, Alberta, Canada. He has split time between industry and academia, holding

positions at Fairchild/Schlumberger Laboratory for AI Research, the Schlumberger Palo Alto Research laboratory, and Hewlett Packard Laboratories in Palo Alto CA, the Air Force Institute of Technology (AF Grad School) in Dayton Ohio, and Intel's Strategic CAD Labs in Hillsboro OR. Dr. Stevens is the principal author of three papers that received the Best Paper Awards. He holds several patents on circuit design and timing analysis, and has implemented in CMOS silicon several large fully asynchronous VLSI chips with significant power and performance advantages over comparable clocked designs. Ken has developed GNU public domain software for an international language spelling checker, and is the co-founder of a software company. He has twice served as technical program chair for the ASYNC symposium and for GLSVLSI. Ken is a Senior Member of the IEEE. His research interests include asynchronous circuits, VLSI, architecture and design, hardware synthesis and verification, and timing analysis.



Alexandre (Alex) Yakovlev was born in 1956 in Russia. He received D.Sc. from Newcastle University in 2006, and M.Sc. and Ph.D. from St. Petersburg Electrical Engineering Institute in 1979 and 1982 respectively, where he worked in the area of asynchronous and concurrent systems since 1980, and in the period between 1982 and 1990 held positions of assistant and associate

professor at the Computing Science department. Since 1991 he has been at the Newcastle University, where he worked as a lecturer, reader and professor at the Computing Science department until 2002, and is now heading the Microelectronic Systems Design research group (<http://async.org.uk>) at the School of Electrical, Electronic and Computer Engineering. His current interests and publications are in the field of modelling and design of asynchronous, concurrent, real-time and dependable systems on a chip. He has published four monographs and more than 200 papers in academic journals and conferences, has managed over 25 research contracts. He has chaired program committees of several international conferences, including the IEEE Int. Symposium on Asynchronous Circuits and Systems (ASYNC), Petri nets (ICATPN), Applications of Concurrency to Systems Design (ACSD), and is currently a chairman of the Steering committee of the Conference on Application of Concurrency to System Design. He is a Senior Member of the IEEE and Member of IET. In April 2008 he was General Chair of the 14th ASYNC Symposium and 2nd Int. Symposium on Networks on Chip, and Tutorial Chair at Design Automation and Test in Europe (DATE) in 2009. He was recently an invited speaker at DDECS 2010, KTN event on Power Management in 2010 and DATE 2011, where he spoke on 'Energy-Modulated Computing'. He is a visiting professor at Technical University of Vienna. He was on advisory board of Elastix Corp in 2007–2011.