Testing with the LV-500

- Tektronix LV-500
- Built in 1989-1991
  - I.e. Ancient technology!
  - eBay is a good source for spare parts these days…
- Specifically designed to be a stand-alone tester for ASICs
  - I.e. More testing features than a basic logic analyzer

Flavors of LV500s

- LV514
  - 192 test channels (12 sectors)
    - 160 are usable (two sectors are bad)
  - Pre-wired test card for class chips
  - *(should really be called LV513, but that's a long story)*
- LV512
  - 128 test channels (8 sectors)
    - All channels are usable
  - Used mostly for tutorial purposes
    - No pre-wired class chip test card yet…

What's an ASIC Tester?

- Ours is built on a Tektronix DAS 9200 logic analyzer platform
- The main differences are in the test head, the pattern/error cards, and the Schmoo
  - The test head has up to 256 bi-directional pins where each pin has programmable electronics
    - voltage drive, current drive, voltage sense, etc.
  - The pattern/error cards store and compare the test vectors at up to 50MHz
    - fast for 1989!
  - A Schmoo lets you run repeated tests while the tester alters one or two independent variables like threshold, delay, cycle length, voltage, etc.

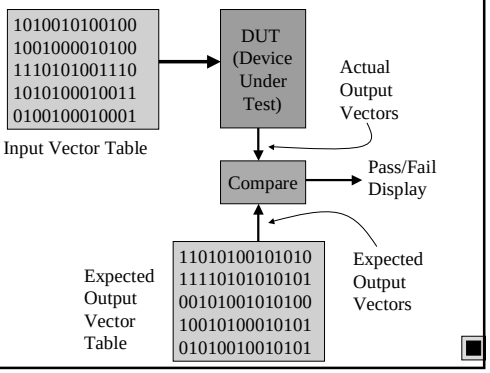
LV514

Flavors of LV500s

- Common Features
  - Test speeds up to 50MHz
  - Up to 64,000 unique test vectors
  - Network connection for uploading tests
    - Thinlan ethernet
  - 8 Meg of RAM
  - 21 or 43 Meg hard drive
  - 5.25 floppy (1.2M floppy)

LV512

The Big Picture



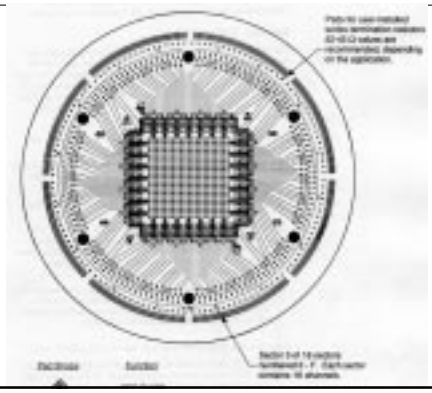
Tester Channels

- The 256 possible pins (channels) on the test head are grouped into 16 “sectors” labeled 0-f
  - Each sector has 16 channels
  - Labeled sector.channel (I.e. 0.2, d.3, a.c)
- On each cycle, each channel may be either a “force” channel or a “compare” channel, but not both
  - If you have bi-directional pins on your chip, you need to define which are inputs and which are outputs on each cycle!

The More Detailed Picture

- Conceptually this is simple, in practice there are lots of details…
  - Define the input and expected-output vectors
    - Can do this using your Verilog simulations
  - Define which signals are inputs and outputs on your chip
  - Define how those signals are mapped to tester channels
  - Wire up the DUT card so that those channels map to your chip pins
  - Define the timing and electrical characteristics of your test

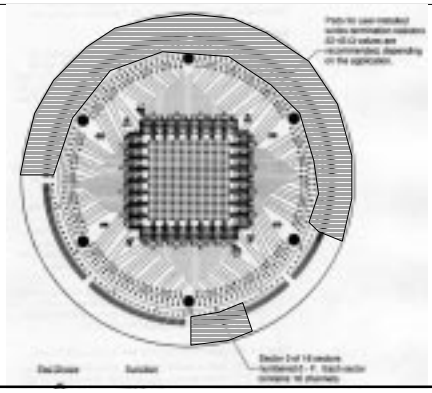
DUT Card



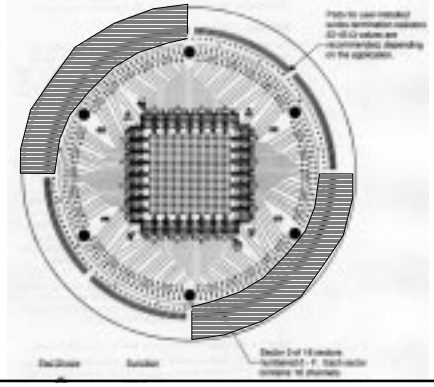
Three Essential Parts of a Test

1. A properly wired DUT (Device Under Test) card
   - This electrically connects each of your chip pins to the correct tester channels
2. A properly configured LV-500
   - Configure the timing of when inputs are applied, when outputs are checked, what the voltages and currents are, etc.
3. A complete set of test vectors
   - Vectors are applied and checked on each cycle
   - “Force data” are inputs to your chip
   - “Compare data” are expected outputs from your chip

LV514 Usable Channels



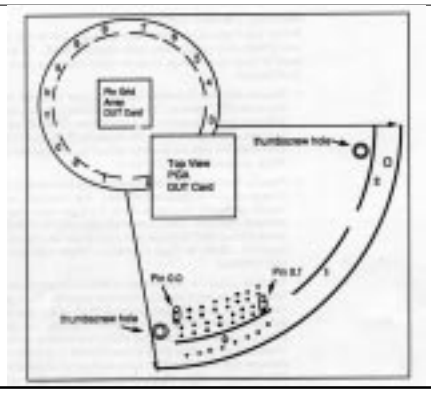
LV512 Usable Channels



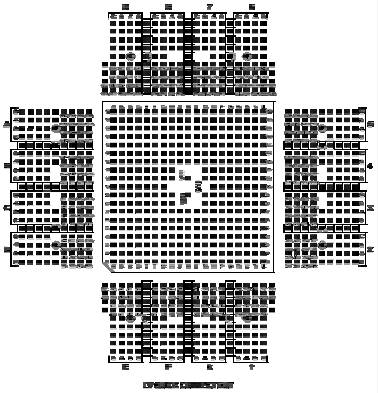
Wiring the DUT Card

- Essentially two choices:
  - Solder wires on a PGA DUT card
    - Remember that VDD and GND are not connected to tester channels
    - Probably only want to do this once for the whole class
    - Which means standardizing VDD and GND!
  - Use a “Quick-Connect” card
    - Uses 3M Scotch-Connect to wire (using wire-wrap wire) from the tester channels to the chip socket
    - Can also use quick-connect for VDD and GND

DUT Card Sectors & Channels



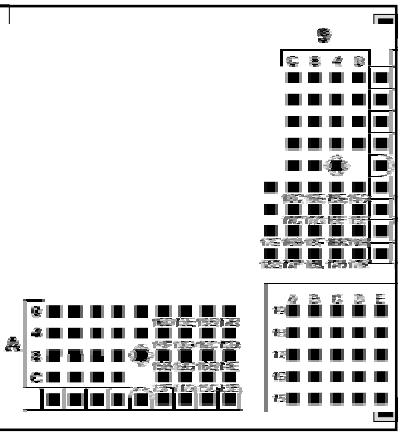
Quick-Connect DUT Card



DUT Cards

- The DUT cards are how you wire from tester channels to chip pins
- These cards also have VDD, VTT and GND power supply connections
  - VDD and VTT are two independently controllable power supply voltages

Quick-Connect DUT Card



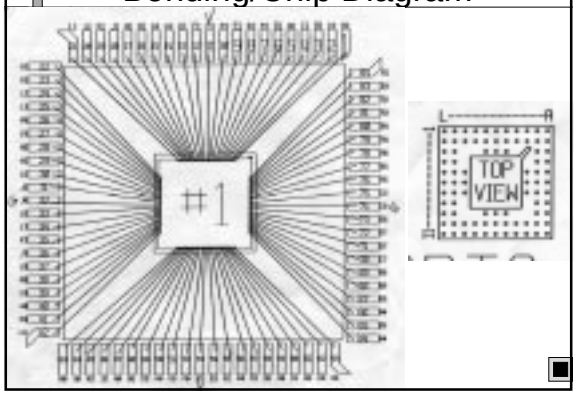
Knowing What to Wire

- A “Bonding Diagram” is a picture that shows how your chip was bonded to the chip frame
- It also shows how the chip frame is connected to the chip pins

Class DUT Card

- Pre-wired for class chips
  - 84 pin PGA with specific VDD and GND placements in the pad ring
  - /usr/local/contrib/elb/lv500/DUTmap.txt

Bonding/Chip Diagram

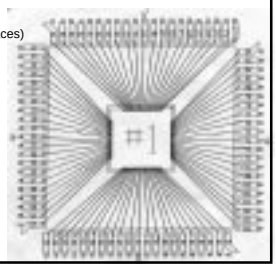


DUTmap.txt

PAD-PIN-TESTER CHANNEL MAP FOR CS/EE 5710 DUT CARD

Pad locations are taken from MOSIS bonding diagram
PGA locations are taken from 84pin PGA bonding diagram
Tester channels 6,7,8,9,A are used. The notation is sector.channel
Vdd and GND connections are as per 5710 standard pad frame

PAD	PGA	TESTER SIGNAL sec.chn	NAME (no spaces)
1	B02	6.C	
2	C02	7.7	
3	B01	6.B	
4	C01	7.6	
5	D02	7.D	
6	D01	7.C	
7	F02	GND	GND
8	E02	8.1	
9	E01	8.0	
10	E03	8.7	
12	F01	8.6	
13	G01	8.A	etc.…



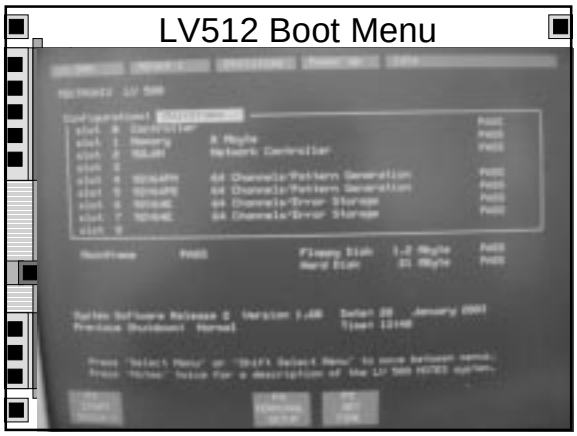
Map Your Pins to Channels

- Pick tester sector.channel assignments for each of your pins
  - Signals that need the same voltage characteristics should be grouped in the same sector
    - Each sector gets common voltage ranges
    - More on this later…
  - Signals that need the same timing should be grouped in the same quadrant
    - Sectors 0-3, 4-7, 8-b, c-f are the four quadrants
    - More on this later…
  - Wire things up!
    - Remember to keep a list of what you’ve wired!

Finished DUT Card

- Now you have part 1 – a wired DUT card that connects your chip to the tester
- On to part 2 – configuring the tester…

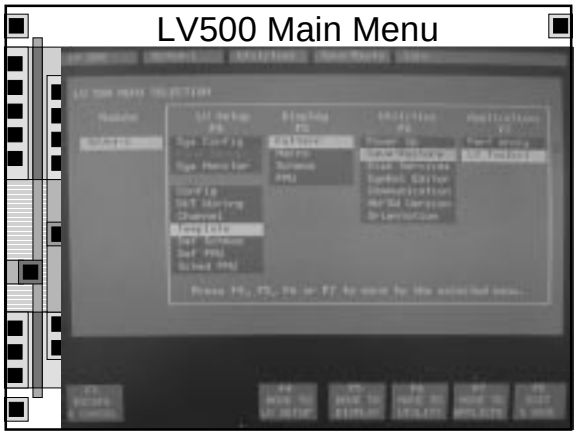
LV512 Boot Menu



Important Menu Choices

- Config Menu
  - Defines voltages for VDD, VTT, GND
  - Defines voltages for two force/compare sets
- DUT Wiring menu
  - Defines how your signals are assigned to tester sector.channels
- Channel menu
  - Defines how your signals are collected into groups (I.e. buses)
    - ALL signals must be a part of some group
    - Groups are assigned to specific timing templates (clock phases)

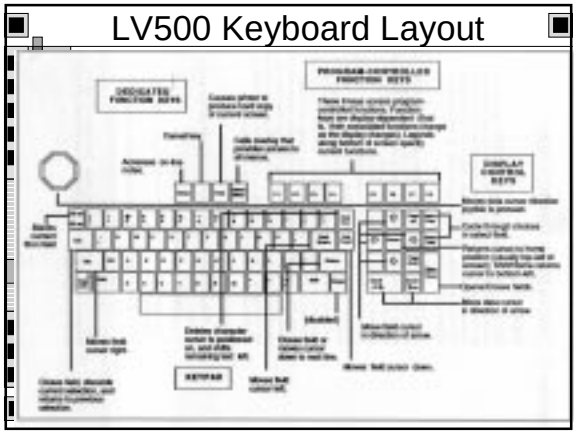
LV500 Main Menu



Important Menu Choices

- Template Menu
  - Defines timing of tests
    - When to force data?
    - When to compare data
    - When to ignore data?
- Schmoo Menu
  - Defines which variables to vary, and by how much
- Pattern Menu
  - Defines data vectors for each tester cycle

LV500 Keyboard Layout



Basic Procedure…

- Tell tester which chip signals are connected to which channels (DUT wiring menu)
- Combine signals into groups (Channel menu)
- Define timing for each group (Template menu)
  - Only four “clock phases” per quadrant
  - A “template” assigns clock phases to groups, and timing of clock phases…
- Define patterns (Pattern menu)
  - Each pattern starts with a template
  - Includes force, compare, and mask data for each test cycle

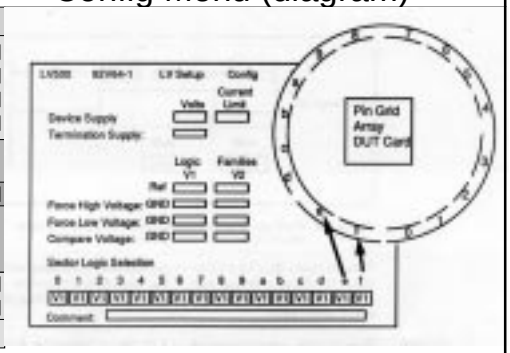
Config Menu

- Defines the electronics for this test
  - VDD, VTT, GND, current limit, etc.
- You can also define two different “force” and “compare” voltage sets for data channels
  - Each sector uses one of these two sets

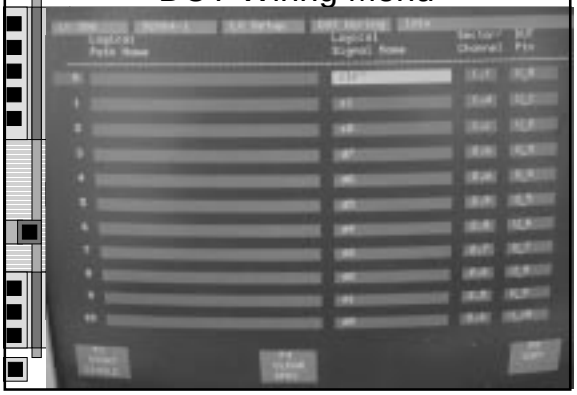
DUT Wiring Menu

- Defines how your signals are assigned to tester sector.channels
  - List signal names
  - Define which tester channels they connect to
  - Optionally define which actual chip (DUT) pins they are connected to
    - This is just a comment for documentation

Config Menu (diagram)



DUT Wiring Menu



Config Menu (LV512)

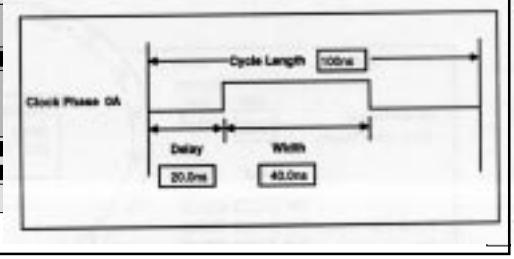
Channel Menu

- Defines how your signals are collected into groups
- EVERY signal must be a part of some group (even single signals)
  - Groups can make data entry and evaluation easier
  - Can define how group data is printed
    - Dec, Hex, Oct, Bin
  - Can specify timing once for the whole group
  - In general, inputs vs. outputs is a good group…
    - Or control vs. data, etc.

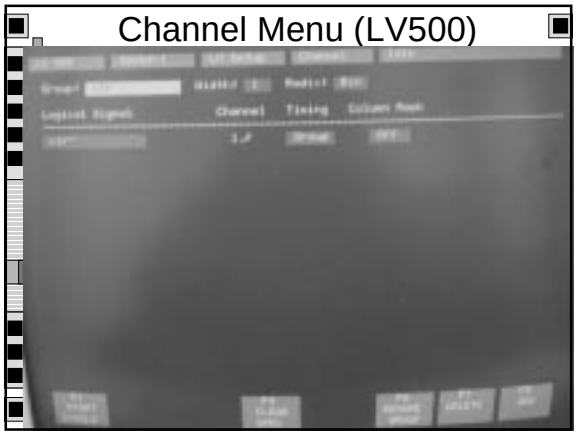
Channel Menu (LV500)

Clock Phases

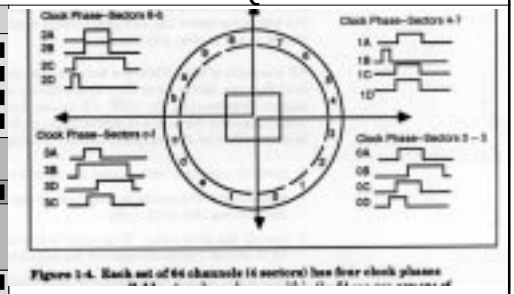
- Cycle Length: 20ns – 496ns
- Delay is delay to Leading Edge
  - Can be 0ns
- Width is delay from Leading to Trailing edge



Channel Menu (LV500)



DUT Card Quadrants



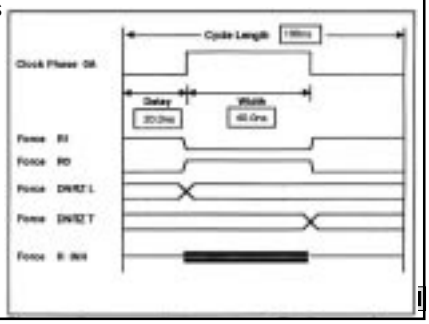
Each quadrant has up to four timing waveforms you can use to control signal timing (called “Clock Phases” in LV500-speak)

Templates

- Templates
  - Defines timing of tests
    - When to force data?
    - When to compare data
    - When to ignore data?
  - Set up using a “clock phase”
    - Bad name – really a timing waveform
    - Defines when things happen in each tester cycle
  - You can define up to four clock phases per quadrant

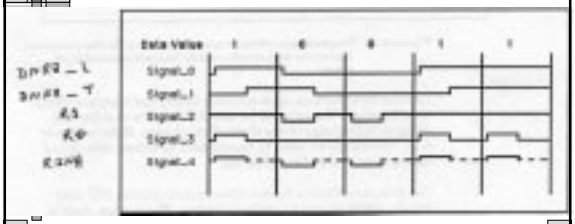
Force Formats

- Within a clock phase, you can define when values are “forced” to your chip in relation to the edges



Force Formats Example

- This is an example of a pattern driven on five consecutive tester cycles with each of the different force formats

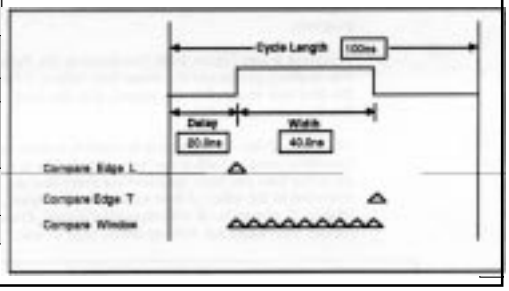


Pattern Menu

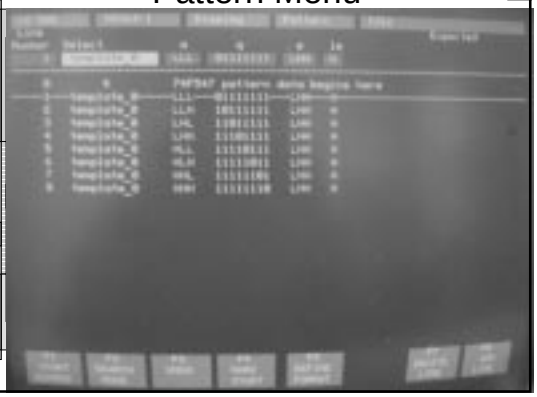
- Defines data vectors for each tester cycle
  - Data for each signal is defined in the data vector
  - Some of those signals are “Force”, some are “Compare” and some are “Mask”
    - These are set in the templates
    - Assign a template to each vector
    - On each tester cycle, the next vector, with that vector’s template, is applied to the DUT and compared

Compare Formats

- You can also define when you Compare outputs in relation to the clock phase edges



Pattern Menu

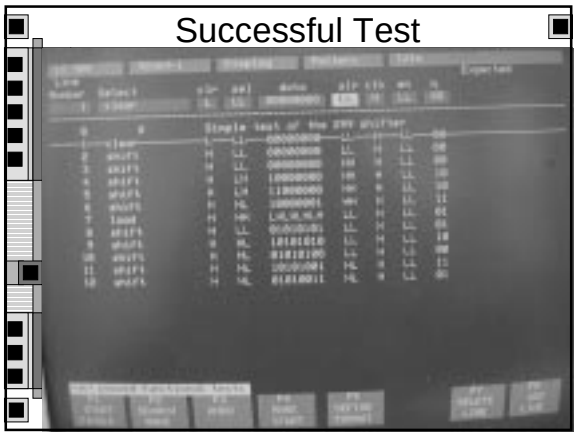


Template Menu

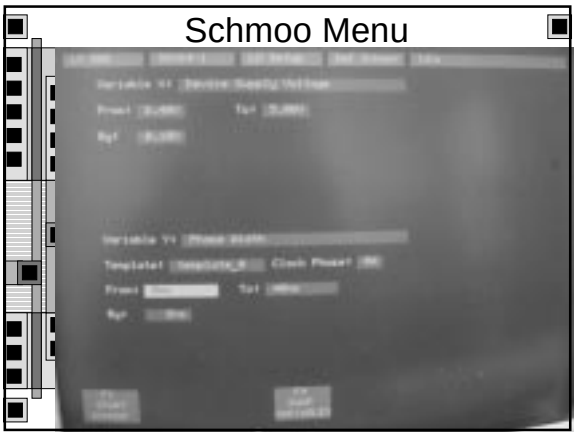
Pattern Display

- The Pattern screen is where you see the results of your test
  - Before the test you can see all the vectors (and their templates) that you will be using
  - After running the test you see the same display with any errors highlighted in red
    - Red means that the output of the DUT didn’t match the expected output vector
  - You run the test with F1-Start (the F1 function key)

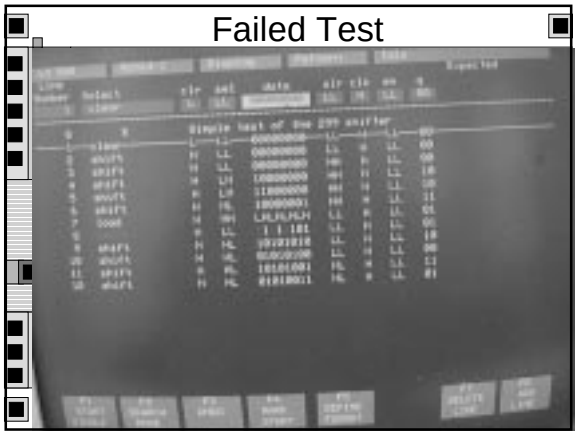
Successful Test



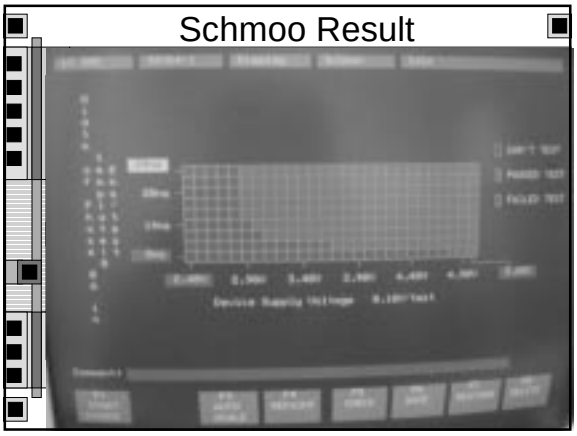
Schmoo Menu



Failed Test



Schmoo Result



Schmoo Menu

- After you have your basic test working, you can run a Schmoo test
  - Repeat the test while changing 1 or 2 variables
    - Variables can be things like VDD voltage, delay time, cycle time. Compare voltage, etc.
  - Generates a graph showing where the part worked or didn't work

Logistics

- The LV500 is old and cranky…
  - Basic rule – if you're not SURE about what you're doing, ask me first!!!!
    - Replacement parts are very hard (impossible?) to find.
  - Leave terminal ON
    - Turn down brightness when you leave,
    - Check brightness when you come into the lab
  - Do NOT turn the LV500 off without good cause!
    - We'll leave the LV512 up and running for tutorials, and then switch to the LV514 when chips come back…

Logistics continued

- Be very gentle with the DUT cards
  - They connect to the machine through elastomer connectors
    - These are basically rubber-like connectors wrapped with wire
    - They are very fragile, and a little worse for wear
    - We have no replacements…
- Schedule some time with me to run tests!
  - Once you've got some LV500 time under you belt you can go it alone…

LV512 LAN Screen

Tester Setup Simplified

- All this stuff can be defined in a .msa file
  - Module Setup, Ascii
  - Each section of the .msa file corresponds roughly to a tester menu
  - You can (fairly easily) write your own .msa file
    - Templates on /usr/local/contrib/elb/lv500/

LV Toolkit Menu (LV512)

Tester Setup with msa Files

- You can ftp to the lv500 and upload the .msa file which defines your test
  - You can ONLY ftp from vlsi-nat.cs.utah.edu so ssh to there first!
  - lv512.cs.utah.edu, lv514.cs.utah.edu
  - No username/password required…
  - Put your .msa file into the Simulation directory on the LV500
  - Convert to tester setup using the LV Toolkit menu

LV Toolkit Issues

- Note that the conversion process goes to an ms_04_4.msp file (or something close to that)
  - You are not allowed to change this name!
  - If you want to save this setup under a different name you need to convert to the standard name, and then save the setup to a new name using the Disk Services menu.
- Once the .msa is converted, you can look at the setup using all the previous menus

Running Tests

- The .msa conversion is a great first step
  - But, after that's running you may want to change things or try new things
    - Like Schmoo, or changing parameters
  - You can change the data using the menus shown earlier
  - You can also save the changed tests into new .msa files
  - And you can retrieve those new .msa files using FTP if you like

Procedure 2

6. Upload the .msa file to the LV500
7. Convert the .msa file to a tester setup file
8. Check all menus to make sure things are how you want them
   1. Config
   2. DUT wiring
   3. Channel
   4. Template
   5. Pattern

Overview

- On every tester cycle the LV500:
  - Applies a set of signals to the DUT
    - The data to "Force" is defined in the Pattern
    - Which signals are "Forced" on this cycle is defined in the template
    - When the data are applied is defined relative to the "clock phase" template
    - The names of the signals and which tester channels they are on are defined in the DUT wiring menu
  - At the right time (defined in the template) the tester captures and compares the data from the DUT
    - Compares against the data in the Pattern

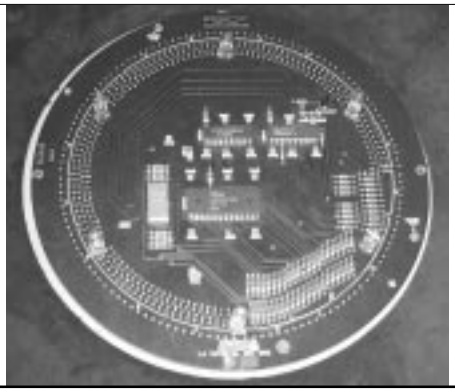
Procedure 3

9. Fix or modify test parameters
10. Run your test
11. Look at the results
    1. Celebrate!
    2. Or diagnose and debug…
    3. Or decide to schmoo to get more info…

Procedure

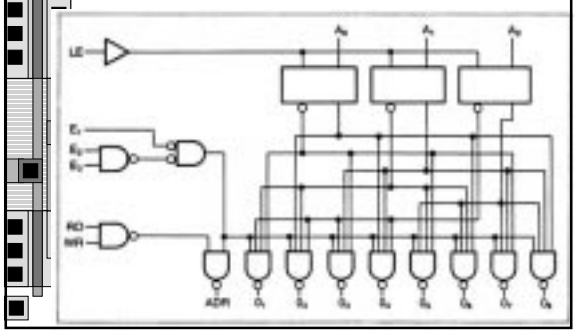
1. Get your bonding diagram and map where your signals are on your chip
2. Decide how those pins will map to tester channels (DUTmap.txt)
3. Decide on timing templates for all signals
4. Generate test vectors that include pin names, templates, and data vectors for every cycle
5. Put it all in a .msa file

Tutorial DUT Card

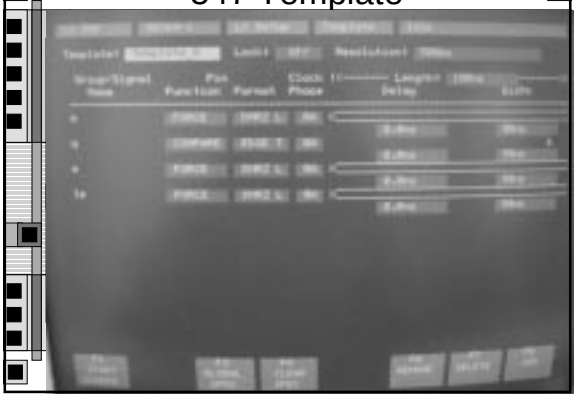


Tutorial 1: 74LS547

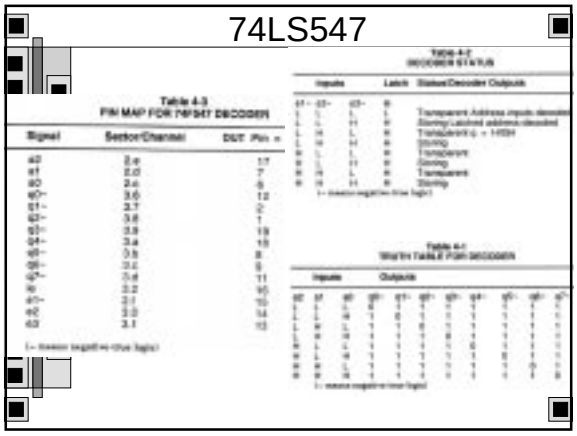
- 3 to 8 decoder



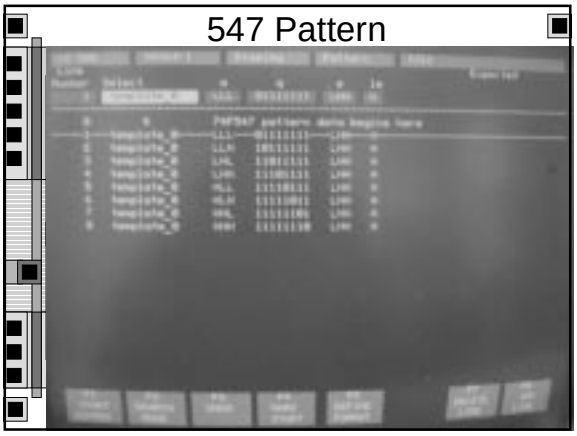
547 Template



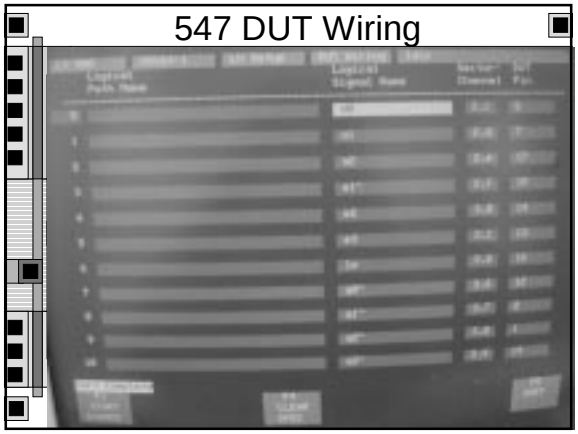
74LS547



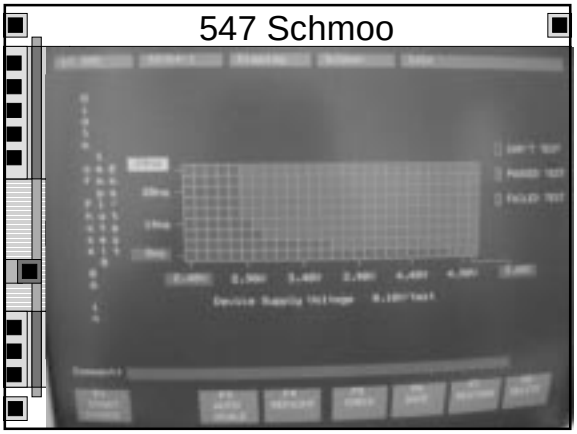
547 Pattern



547 DUT Wiring

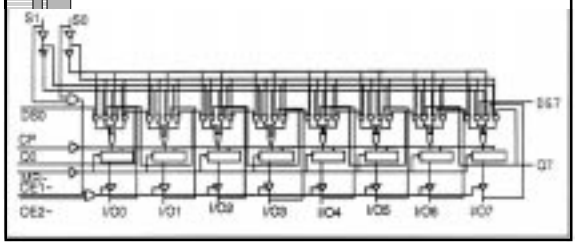


547 Schmoo

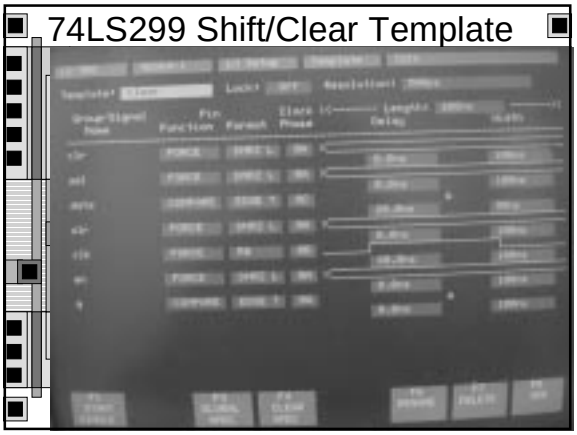


Tutorial 2: 74LS299

- Shift Register, shift L or R, parallel load and output
  - Bidirectional data bus



74LS299 Shift/Clear Template



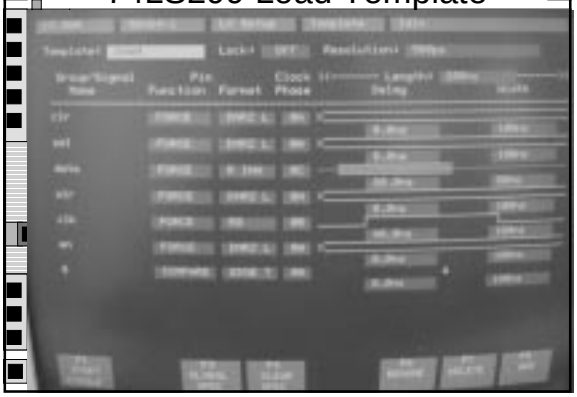
74LS299 Timing

- Control should be set up ahead of the clock
- Data should be sampled after the rising edge of the clock
- Data should be driven after the control is set up
  - Avoid drive fights on bidirectional path

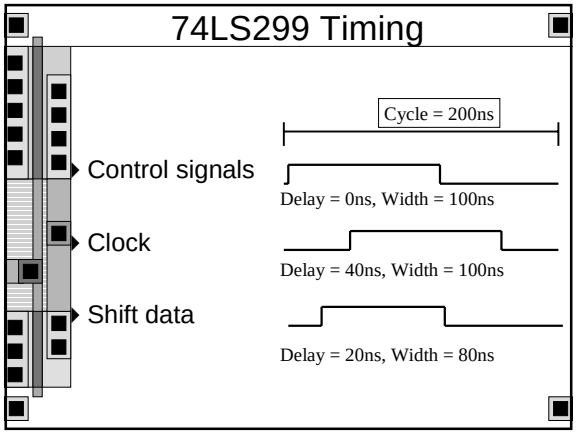
Table 6-I
FUNCTION TABLE FOR 74LS299 SHIFT REGISTER

Inputs				Response
clr-	s1	s0	clk	
L	X	X	X	Asynch Reset:d[7:0]=Low
H	H	H	0->1	Parallel Load
H	L	H	0->1	Shift Right
H	H	L	0->1	Shift Left
H	L	L	X	Hold

74LS299 Load Template



74LS299 Timing



74LS299 Pattern