Testing Report for Emulating Interval Tuning Property of a Neuron Using Domino Gates

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***Abstract*—This report examines the results of the chip fabricated for the project Emulating Interval tuning property[1] of a Neuron using Domino Gates. The testing methods employed for verifying the functionality of the chip are discussed. The test results are shown pictorially and compared with the expected results.**

***Index Terms*—Domino Gate, Interval Tuning Property, Tektronix LV514, Schmoo Test.**

I. Introduction

The project, Emulating the Interval tuning property[5] of a Neuron using Domino logic Gates, provides mechanical understanding of interval selectivity and counting property of the neurons in the nervous system. Neuron in anurans [5] generates a response signal at the reception of optimal pulse intervals over a range of frequencies. The interval counting process gets reset at the reception of pulses which are either Early or Late compared to the optimal pulse duration. In Fig 1, the results obtained in the project are shown. The plot shows, Correct pulse (pulse width- 5ns, Pulse Period- 20ns), Early pulse (pulse width- 5ns, Pulse Period- 23ns), Late pulse (pulse width- 5ns, Pulse Period- 17ns) in four different stages of the design. The output response of the circuit is shown along with window generator output which keeps high on receiving correct pulses.

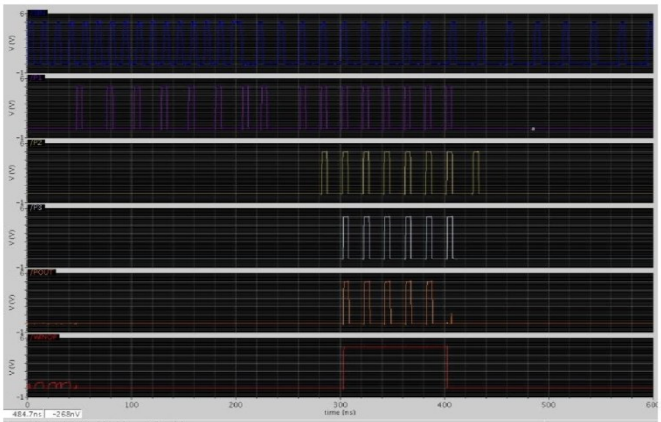

Fig1. Results showing interval tuning property of neuron for Correct, Early and Late Pulse Scenarios

II. Project Specifications

This project implements interval tuning property for four consecutive synapses with correct temporal spacing and order. The circuit responds with a pulse at the end of fourth pulse interval. In case of incorrect temporal spacing and order i.e., either Early or Late pulses, the circuit does not respond. It in turn generates a window pulse indicating the reception of wrong pulse.

Circuit is designed with standard domino gates [6], delay components and combinational logic gates. Sizing of transistors is done to meet the required delay specifications and domino behavior. Single stage detects one input pulse. Four single stages are cascaded in such a way that after four consecutive correct pulses, the final stage produces the pulse output.

The circuit is hand routed since Domino gates cannot be easily synthesized compared to other static gates because of their self resetting behavior. The Core layout is done using Cadence Chip Assembly Router. The Layout is connected to the Pad Frame using which is accommodated in One Tiny Chip Unit (1 TCU).

A. Functionality

Initially an external active high signal is applied to ‘RST’ pin to pre-charge the domino gate. The ‘EIN’ and ‘PIN’ pins are held high throughout the operation and used as inputs only in the first stage. Once the input synapse is applied to ‘SIN’ pin the domino output is pulled down. The response is fed as input to the asymmetric delay which produces delay in the falling edge. The output of the asymmetric delay is inverted and delayed using delay elements in order to produce the pulse output which synchronizes with the next synapse at the ‘POUT’ pin.

Simultaneously, the asymmetric delay output is fed back to the domino gate to pre-charge the circuit for the next synapse. Hence the pre-charging of the domino gate is delayed by required asymmetric delay. Once the domino gate is pre-charged the high signal at the input of the asymmetric delay will be instantly observed at the asymmetric delay output which will produce the required pulse width.

B. Inputs to the Design

The inputs to the design and their status are shown below:-

INPUT	STATUS
EIN	Always held 'HIGH'
SIN	Controlled by User
PIN	Always held 'HIGH'
RST	Controlled by User
WINRST	Controlled by User

Table 1.

In the current design, the inputs EIN or Enable Input, PIN or Pulse Input, are held HIGH throughout the runtime of the design. SIN or Synapse In is controlled by the user. The functionality of the design in testing the three cases Early, Late and Correct pulses are given through SIN input. In the design, the correct scenario corresponds to a frequency of 50MHz. Any frequency below or above this corresponds to Late or Early scenarios respectively. RST or Reset Signal is held HIGH initially for a period of 5ns to activate the circuit and maintained low thereafter. WINRST or Window Reset signal is used to activate the Window Generation Module and held HIGH for the initial 47ns. The supply voltages VDD and GND correspond to 5V and 0V respectively.

C. Outputs from Design

P0, P1, P2, P3 are the outputs corresponding to First, Second, Third and Fourth Stage respectively. POUT correspond to the final response of the circuit which depends on output response of each stage. WINOP is the Window response of the circuit which raises high during the correct pulse detection, else it remains low.

III. Chip Fabrication

The design was fabricated by MOSIS circuit-fabrication service[3], which provides design fabrication for educational purpose. Fabricated designs vary in size, and are measured in Tiny Chip Units (TCU's). Arbitrary numbers of TCU's are not allowed and designs must fit into sizes of one, two and four TCU's.

Since the designed chip contains lesser number of pins and small area it was easily accommodated in one TCU. Designed chip with padded frame is shown in Fig. 2.

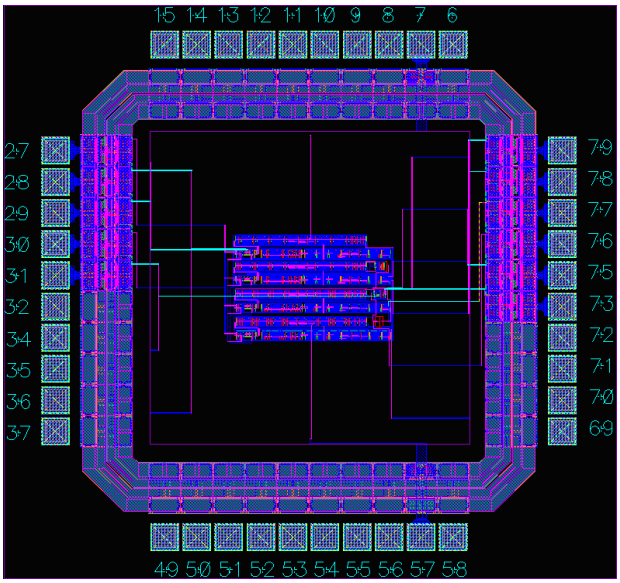

Fig.2 Designed Chip with padded frame

IV. Testing Methodology

The Chip is tested using Tektronix LV500 machine built in 1989. It runs at speeds up to 50MHz and can generate up to 64,000 unique test vectors. There are two flavors of LV500 namely LV512 and LV514. LV512 contains 128 test channels divided in to 8 sectors whereas LV514 contains 192 test channels divided into 12 sectors. LV512, to which the decoder chip is fixed, is used for tutorial purpose. After successfully passing the tutorial, the fabricated chip is placed on LV514 shown in Fig.3 and is ready for testing.

Fig.3 LV514 Test Equipment

A. *Steps for Testing*

1. DUT wiring is essential to indicate how signals are connected to various sectors and channels of the tester.
2. All the test signals are to be divided into groups. Signals of similar characteristics (same phase and period) can be placed in a single group.
3. Timing of test signals, which are used to force, compare or ignore (mask) the data are applied by choosing templates from template menu
4. Data vectors applied for each test cycle can be seen in Pattern menu.
5. Finally, the test [2] is run and results are displayed in the Pattern menu.

If the generated outputs (output of DUT) match with the expected outputs, message appears on the screen as "All functional tests passed". If the comparison fails, the error vectors are highlighted in red with the error message "Failed to pass Functional tests".

The test patterns can also be applied directly by creating .msa file and importing it in to the tester from LV514.cs.utah.edu server through ftp. It automatically configures the setup menus and test can be directly run.

B. *Schmoo Plot*

After verifying the basic functionality of the chip by running tests, Schmoo test is run. Schmoo test is run in order to determine the functionality of the chip by varying external parameters which are functions of voltage and time. The output signal template is chosen initially and Schmoo is defined to choose parameters such as supply voltage, forced supply voltage, cycle length, phase width and phase delay. The selected X and Y-axis parameters are plotted against each other for a specific period and range. The Generated graph shows where the chip worked or not and is divided in to three regions:-

1. Failed test – indicates the region where device failed to work. This region is highlighted in Red.
2. Passed test - indicates the region where the device is functioning properly. This region is highlighted in Blue.
3. Can't test – indicates the region where tester cannot test the functionality of the device. This region is highlighted in black.

V. TEST RUN DESCRIPTION AND RESULTS

Current Chip design contains five input pins and six output pins. They are divided into ten groups (groups with same cycle phase are placed together). The test patterns (signals containing cycle time generated over a specific time interval) are chosen according to the requirement and forced through the input pins. The output signals are set in compare mode and their timing is applied to match the expected results.

Two different templates are used to set the pattern. The first template 'tmp0'with cycle length 24ns and pulse width 8ns is used to apply the reset signal to the design and all other pin groups are configured according to the requirement. The second template tmp1 with pulse width of 8ns and cycle length of 24ns is used to apply the synapse input through the pin SIN and all other pins are configured according to the requirement. The input pins EIN and PIN applied are maintained HIGH in both the templates. The RST signal is set high in tmp0 and maintained low in tmp1. The SIN or Synapse signal cycle length is set to 24ns with a width of 8ns in both the templates tmp0 and tmp1.

The outputs P0, P1, P2, and P3 are taken from first, second, third and fourth stages respectively. The output at P3 is considered to be the final response. If the frequency and phase of the outputs generated at each stage matches, the output response is obtained at P3.The tmp1 is repeated in the pattern menu to verify the outputs of the design at each stage. The compare signals for the outputs P0, P1, P2 and P3 are chosen in each of the template to compare the expected outputs with the obtained outputs. The test is run and the obtained result is shown in Fig.4. "Passed Functional Tests" appears on screen when the expected outputs match with the desired results.

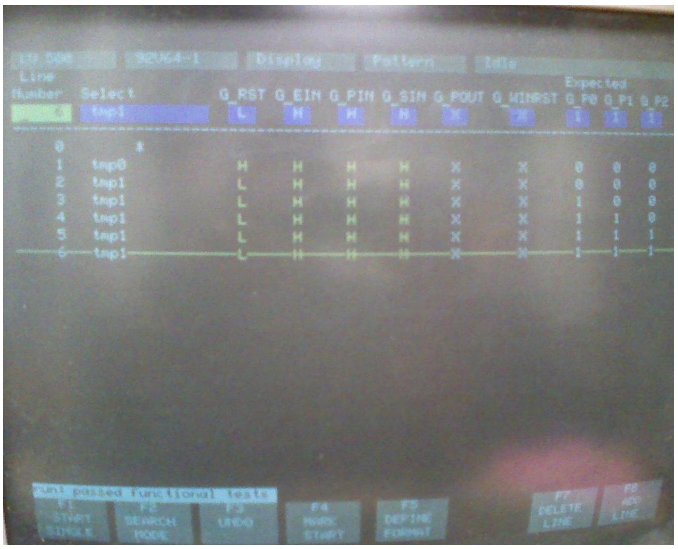

Fig.4 Pattern display of LV514 screen showing the status of test run as "Passed"

For the late scenario, we have configured the inputs accordingly with increased cycle length of 28ns by maintaining pulse width of 8ns. The compare outputs for the correct scenario were maintained same in this case. When the test is run the status message is obtained as "Failed to Pass Functional Tests" with the error vectors in red as shown in Fig.5. The behavior is as expected since during the late scenario the outputs at each of the stages are out of phase and hence doesn't match with previous outputs. Hence the basic functionality of the design is verified successfully.

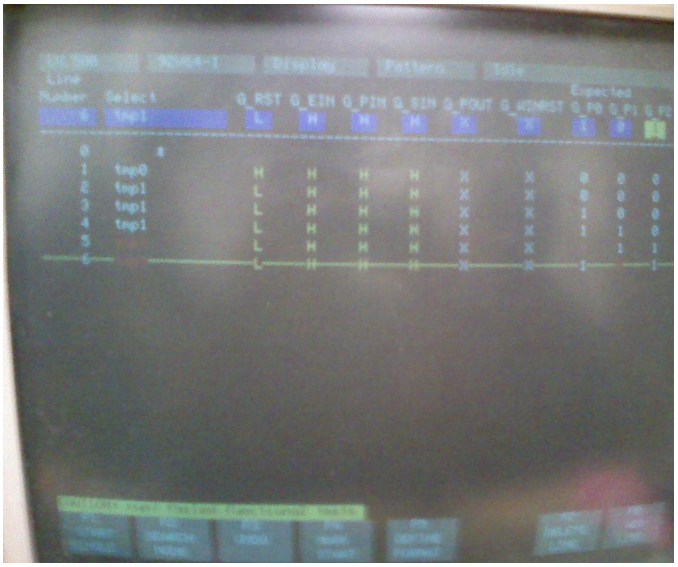

Fig.5 Pattern display of LV514 screen showing the status of test run as "failed"

Schmoo test [1][2] is run for the templates tmp0, tmp1 where the circuit behavior is tested. Forced high voltage (V1) over the range 2.20- 4.65V on Y-axis is plotted against Cycle length over the range 24 - 44ns on X-axis. The resultant graph is shown in Fig.6.

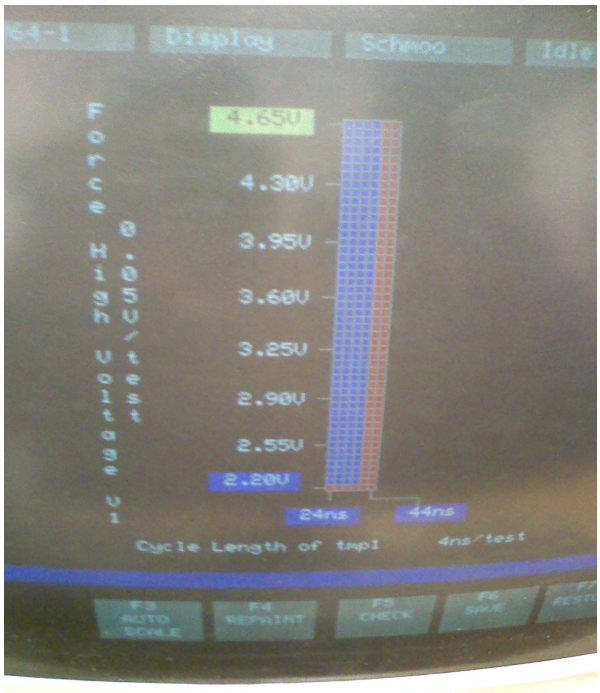

Fig.6: Graph showing Schmoo test against Forced high voltage (V1) and phase delay from LV514 tester monitor.

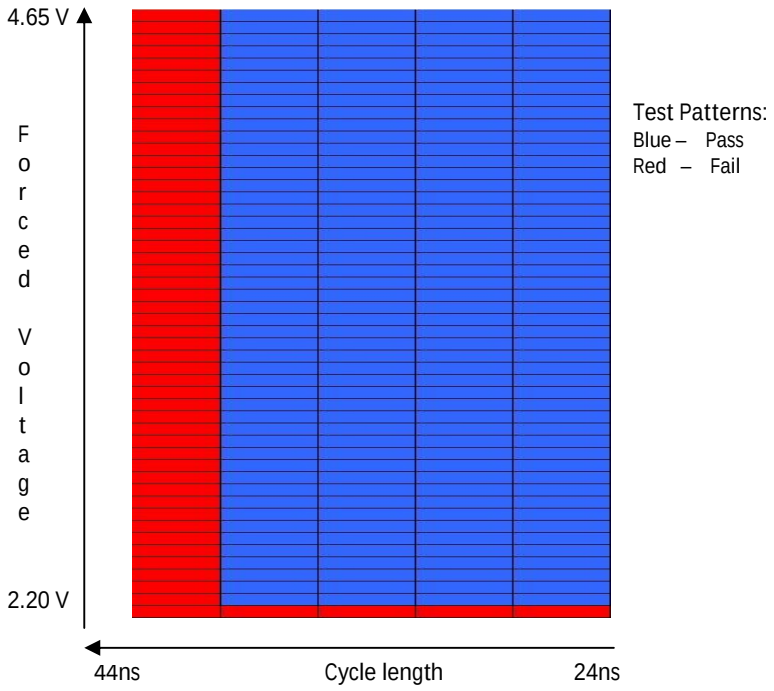

Fig.7: Graph showing Schmoo test against Device Supply voltage and phase delay (Same as Fig.6 except cycle length increasing from right to left)

Fig.7 shows a Schmoo graph plotted Cycle length against Forced high voltage (V1). From the plot we can observe the failed tests are registered when cycle length was more than 36ns. This depicts our late scenario/incorrect pulse scenario in our design where the expected output fails to match beyond the cycle length of 36ns. Also we can observe when the forced high voltage was below 2.25 volts, failed tests were registered because of the increased delays.

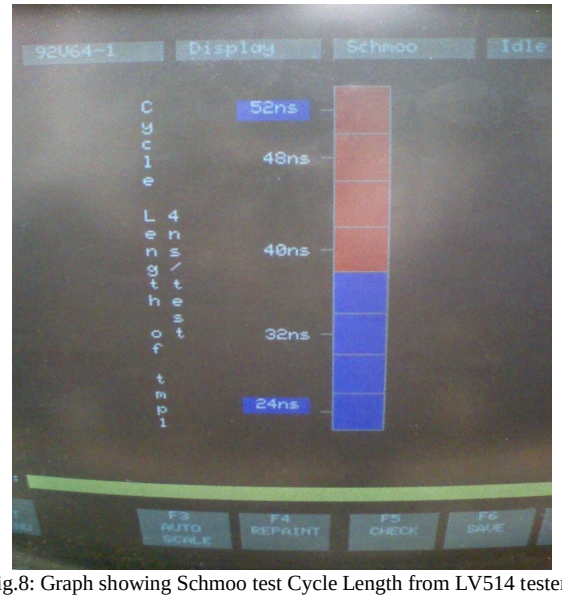

Fig.8: Graph showing Schmoo test Cycle Length from LV514 tester monitor.

Fig.8 shows a Schmoo graph plotting cycle length along Y-axis over the range from 24ns to 44ns. From the plot we can observe the registered pass and failed tests when cycle length is below and above 36ns respectively.

VI. Problems encountered

The testing strategy includes three test cases Early, Correct and Late Scenarios. Early scenario could not be tested because the tester runs at a maximum speed of 50MHz and cycle lengths of inputs cannot be below 20ns.

VII. Yield

Five Chips were received from MOSIS circuit-fabrication service[3]. Each Chip was tested individually to verify the functionality. Chips were tested at an operating speed of 50MHz. Four chips were able to produce expected results meeting the functionality requirement. One of the chips could not meet the expected functionality since it generated no results during testing. Hence the expected behavior of the project design was observed through the fabricated chips.

VIII. Conclusion

The chips were successfully tested for their functionality. All the test signals were configured in the menus and applied to the design. Schmoo test was run and generated binary file was retrieved from the server through ftp. The .msa file generated by converting the LV setup containing the configured menus was retrieved through ftp.

ACKNOWLEDGEMENT

We thank MOSIS Organization for fabricating chips and giving us an opportunity to test our designs in real time environment. We take this opportunity to thank Dr. Kenneth Stevens for his guidance and support throughout the course of this project.

References

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Appendix

Bonding Diagram: