ECE/CS 5710/6710 – Digital VLSI Design
Design Requirements

1 Introduction

There are many options that you can use to design your cell. While the design rules can not be violated, there are many options that you have for implementing your design. This includes cell height, width, transistor directions, etc. We want to encourage design creativity, while also helping you to be productive in your design and layout. The following rules will significantly help you be productive in this class.

2 Specifications

Following are the specifications that will be used in this document in regard to cell design.

- **Cell Origin** The origin of the cell is defined at location 0,0 of the layout. For layouts created in this class, the origin at 0,0 will have a `SUBTAP` cell placed on the origin

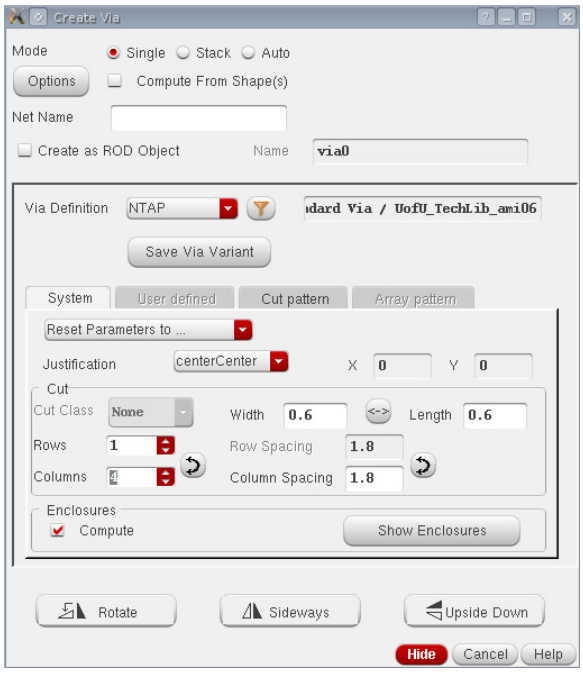

Figure 1: The Cadence Create Via menu - note the ability to array them.

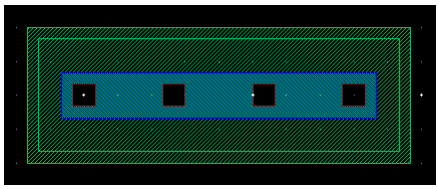

Figure 2: An array of NTAP vias in a one by four configuration

with the center of the contact cut of the origin at the origin. (You can grab a subtap for insertion in Virtuoso with 'o' or create | via.)

- **Cell Height** The height of the cell will be 27.00μm. An NTAP cell will be placed where the center of the contact cut is at location 0,27.
- **Cell Width** The width of the cell must be evenly divided by 8 λ, or 2.4μm per horizontal unit. This is the spacing that is achieved by creating an array of SUBTAP or NTAP cells, and measuring the distance between the center points of the contacts. You can array a set of vias in the Create Via menu, shown Fig. 1. In this example, there are four columns specified in the via that will create a 1×4 array of NTAP vias shown in Fig. 2. This would define a 4-unit wide cell.
- **Labels** Labels in your design should be placed inside the cell. So the label origin location should be on or inside a bounding box from the cell origin, to the cell height and cell width.
- **Supply Rails** Your power and ground lines should run horizontal in your cells, with Vdd on the top, and Gnd on the bottom.

There are two key rules that need to be obeyed to facilitate cell library characterization as well as enable your cell to be properly placed and routed:

1. **Pin Location** Each pin in a cell must be placed on a 2.4μm $\times$ 3.0μm grid in order to be correctly characterized. We have provided a grid template in order to help you properly place pins in your cells on the grid. Without this you will almost certainly run into trouble when characterizing your cells.
2. **Pin Configuration** Pins for your cell library will be on either the first or second metal layer. Each pin should be 0.6μm $\times$ 0.6μm (2 λ square). The center of the pin will need to be placed on the axis of the grid locations.

A grid template has been created to help you design and place your power and ground rails, your well and substrate taps, and your input and output pins. To use this template, you will need to include the grid in your library path. In Virtuoso, open the Library Path Editor

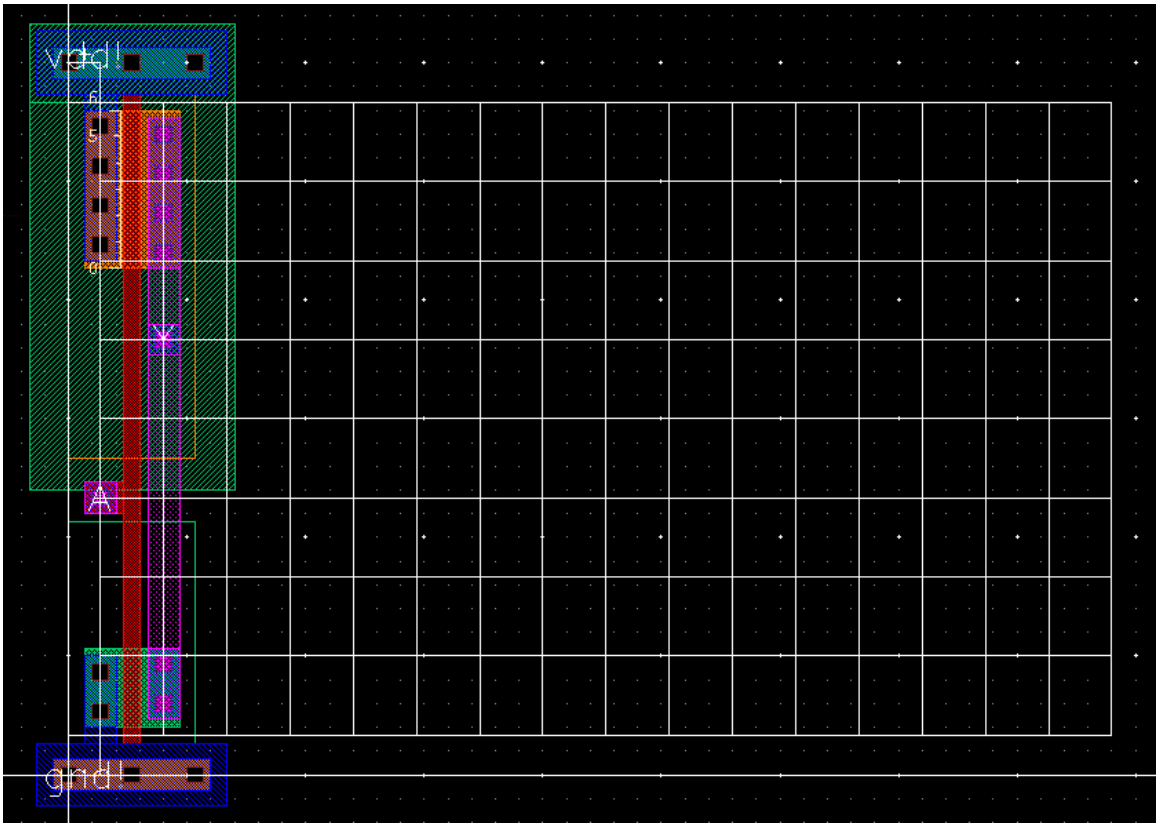

Figure 3: Inverter Example, with transistors that are twice the minimum.

(Tools | Library Path Editor). At the bottom of your list of libraries, create a library named `gridTemplate`, with the path:
`/uusoc/facility/cad_common/local/Cadence/lib/OA/gridTemplate`

When you save the change, you will have a new library called `gridTemplate` with a cell named `gridTemplate`. When you open up a new cell, first insert the `gridTemplate` cell at the origin 0,0 of the new layout. Then start building your cell by placing substrate and well taps at the cell origin and with the correct cell height. When you define and place your pins, place them centered at the cross hairs of the grid template.

Following these rules will reduce frustration and allow you to quickly build and characterize your library. Fig. 3 shows an example of an inverter that is twice the minimum size, or $W = 3\mu \times 6\mu$.