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Evaluation of Integrated Circuit Power Supply Noise with Two-Phase Analysis

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ABSTRACT

Current process scaling allows for the placement of an exponentially growing number of transistors on an integrated circuit. This has resulted in transistors which are faster and operate at lower supply voltages, but with higher overall chip power. This results in substantial noise in the power delivery both on-chip as well as across the package, which results in loss of performance and reliability. Evaluating the supply integrity is beyond the capability of traditional simulation methodologies due to both the number of transistors, as well as passive components (resistors, capacitors, and inductors), in the power delivery system. Two-phase analysis is a method used by the industry for estimating the magnitude of the variance in a circuit's power delivery network. This project will evaluate the noise induced by two modern packages used by Micron Technology and will present the results of several experiments on the power delivery system. In addition, some comparisons will be made between the accuracy of the simulations performed with Synopsis HSPICE (the "golden" reference) and two-phase modeling employed by Synopsys HSimPlus.

I. INTRODUCTION

Lower power supply voltages have put today's large Integrated Circuit (IC) designs at an increased risk of failure due to unpredictable voltage drops in the circuit's supply. As IC operating frequencies and signal data rates continue to increase, power delivery is quickly becoming more complicated. The power delivery network (PDN) should provide consistent and accurate power to the circuits and it has been shown that a PDN is a critical design component in large designs, especially for high performance systems [1].

The purpose of a PDN is to supply power to all devices in a system. The ideal function of the PDN is to deliver clean power to the ICs, provide low impedance, low noise reference paths for signals and to reduce excessive Electromagnetic Interference. When a PDN is unable to provide clean power and low noise it behaves more like a non-ideal PDN with disorderly noises. Unfortunately, the PDN must address ever-restricting specifications caused by lower voltages, smaller timing margins, faster frequency and time-domain performance metrics and multiple source data management.

Circuits need to be analyzed to ensure they will operate reliably, and as such, simulations must be accurate. One of the main problems with the simulation of modern circuits is that extremely large amounts of time are required to fully simulate billions of transistors on circuits completely. Industry has been using a method called “two-phase" or “two-pass” power supply noise analysis to address this. Two-phase modeling leads to reasonable simulation times while providing a high degree of accuracy. The two-phase analysis uses a combination of dynamic and static methods to create a analysis method that has the strengths of both.

In this project, a tool flow for designs were developed, which were then implemented into test circuits utilizing IBM's 65nm 10sf process. The two Micron-provided PDN packages are compared against each other to determine their affects on power supply noise. HSimPlus was selected to implement the two-phase methodology, which would be able to run simulations that would be compared against HSPICE. Using both simulators in combination with the provided package models, simulation results of several different circuit models were compared to determine HSimPlus accuracy and simulation speed.

II. Tool Flow

Two-phase modeling can be tested using simple circuit designs. Due to the complexity of memory circuits HSPICE simulations are unrealistic because they require more time and memory than is available.

Test circuits were first designed in Verilog and then converted to SPICE format. Each test circuit tests different aspects of HSimPlus' two-phase model. ModelSim SE verifies the logic of each test circuit. Conversion of Verilog test circuits to HSPICE is a complex process. First the behavioral Verilog file is converted to an registered optimized Verilog file. Then the logic of the circuit is mapped and synthesized to actual components from IBM's process libraries to create a structural Verilog file. The structural Verilog file is then converted to spice format using Mentor’s v2lvs utility. After the conversion to SPICE format a few changes to the power nets are completed using script files.

HSPICE and HSimPlus both require a control file for simulations. Items found in the control file include: ".include" statements referencing the libraries and circuit modules, instantiations of various circuits, definitions of voltages, input stimulus, simulation directions, output measurements, and optional parameters (ex. HSimPlus precision parameters).

Micron provided a single-layer package (SLP) and a two-layer package (TLP) to aid in the simulation of the test circuits. The packages model the resistive, capacitive, and inductive (RLC) impedance that exist in real world

circuit applications. The power and ground nets for the circuits connect through the packages to ideal power and ground sources. In order to simplify the control file designs, input stimulus and output connections do not route through the package. Unless otherwise noted, a single power pad at the die side provides power to the circuits.

III. Comparison of the Two Package Models

Comparison of the two package models is done by connecting a simple 16-bit ALU circuit. The ALU has two 16-bit input lines, a two bit control line, a clock input and a 32-bit output line which is assigned the result on the rising edge of the clock. For a better illustration of the ALU design, refer to figure A1 in the appendix. Depending on the value of the control line, the ALU performs an add, subtract, multiply, or divide.

Simulations using the package models can then be compared to a simulation of the circuit performed without the package (WOP). The output from the WOP simulation is a near ideal square wave with 1.2V amplitude as seen in figure A2 in the appendix. The output from the SLP simulations shows a variance of up to 0.32V in comparison to the 1.2V WOP simulation. On the other hand, the output from the TLP simulations shows a smaller 0.28V variation. Figure A3, in the appendix, shows a direct comparison between the three simulations: output from the SLP simulation, output from the TLP simulation, and output WOP simulation. The threshold voltage of the transistors of the 65nm library is approximately 0.25V. If the oscillation from the normal voltage dips below this value, the circuit would be considered unstable and require alteration. This variation is potentially troublesome if, instead of a 1.2V power input, the circuit experiment provides a 0.7V input. In such a case, the oscillations place the circuit input too close to the threshold voltage of the transistors. This may result in unpredictable output as some transistors leave the active mode of operation.

The oscillations in the power input signal translate into oscillations in the output signal. The SLP causes a delay of 0.11ns on the rise of the output signal, while the TLP produces a much smaller delay time. One interesting difference between HSPICE and HSimPlus simulations using the TLP is a phase difference of 0.19ns, as is depicted in figure A4 from the appendix. This is a difference large enough to significantly alter the output of the circuit; causing the output signal to rise slightly behind the signal produced by HSPICE.

IV. Package Power HSimPlus Simulation

One interesting fact about the package is how many more power lines there are than other signal lines. By altering the simple ALU circuit to use eight power lines instead of one it is possible to determine the effects that multiple power lines have on the ALU. Each sub-circuit is divided up to receive its power from one of the 8 sources. The simulations from the split power (SP) show a significant increase in the frequency of waveform of the power input. The SP simulations also show a significant decrease with a magnitude of 0.4V peak to peak when compared against the non-split power (NSP) experiment. A direct comparison of this result can be found in figure A5 in the appendix.

This smaller variation on power input and higher frequency also translates through to affect the output signal. As can be seen in figure A6 in the appendix, the output signal shows a 0.2V smaller magnitude of variation as well as a higher frequency. For complex memory circuits, the stability of the PDN is important. Voltage variations in the PDN can introduce signal delays and can cause the circuit to become unstable if the variations are large enough. Using multiple power delivery lines can significantly reduce the magnitude of the oscillations in the power delivery network.

V. HSimPlus Simulation Flow

The HSimPlus' control file contains the signal and power interconnects, circuit netlist, and device geometries. This information is taken and run through many steps during the simulation. The first simulation step is parsing the netlist. The device geometries and system interconnects are used to back annotate the circuit. Using the back annotated data HSimPlus checks to see if a reduction in the RC and/or power net is necessary. HSimPlus will reduce the signal and power nets through a Power Net Reliability Analysis (PWRA) or signal net reduction respectively. The reduced nets are then stored hierarchically in a database. This database provides the information to initialize and run the actual simulation providing the output.

HSimPlus implements its own techniques and proprietary algorithms for system two-phase modeling. In the first phase the circuit is decoupled and a simulation is performed using the circuit's pre-layout netlist. The RC networks and power nets are then connected and HSimPlus models the devices as current sources. Error can be introduced at this step with the reduction of multiple physical nodes down into smaller logical nodes. The second system phase is where the grunt work is done. The power nets are simulated using the created currents injected into the simulation. The PWRA analysis is started and completed during the second system phase.

The PWRA is a two-phase analysis run on the power net. The first phase of the PWRA is to reduce the power net which enables a transient simulation to be run. This is done by breaking the large power nets into multiple smaller sections with smaller component counts. During the transient simulation the dynamic voltage (IR) drop across components is calculated. The second phase of the PWRA measures the node voltage and current through each branch from the original unreduced power nets.

The final phase of the system analysis includes the node voltages and branch currents created during the second phase of the PWRA. Simulations are then run with the current sources included from the first phase of the system two-phase modeling. This is a faster way to simulate and analyze large circuits with high transistor counts. It does introduce chances for error that can change the functionality of the circuit and this error should be kept in mind during simulation of circuits since the actual output can vary to some degree from the simulated output.

HSimPlus then implements hierarchical netlisting during simulation. This reduces the amount of memory dedicated for the netlist allowing more memory to be used towards the actual simulation. This netlisting works by storing the circuit components in different locations. These netlists are stored according to their location in the circuit. Figure 1 below shows a simple six transistor circuit design blocked off into hierarchical netlisting sections. The circuit contains three parts X1, X2, and X3. Each section is compared to the other circuit blocks to see if there are any repeating blocks. In figure 1 X2 and X3 have the same input signal and same component dimensions, X2 and X3 will be stored as one netlist with two different references. Block X1 will be stored separately so that if X2 or X3 need to be called the computer will not need to sort through excess data. This hierarchical netlisting is what makes HSimPlus capable of simulating large circuit blocks, groups of interacting circuits, and entire chip designs.

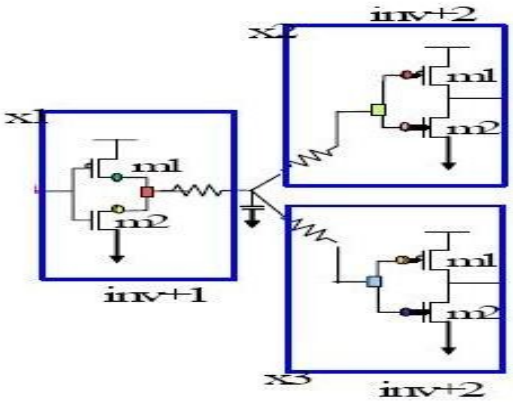

Fig. 1. Netlisting a Six Transistor Circuit [2]

Parasitic RC's are created during the layout of a circuit. These parasitic values must be included in order for the circuit simulation to be as correct as possible. HSimPlus can back annotate these parasitic RC's in two different ways: with Post Layout Acceleration (PLA) on or off. The PLA is a tool that uses algorithms derived by Synopsis to make it possible to fully back annotate a circuit and keep the netlist in the preferred hierarchical order. If the PLA is turned on then the RC's will be netlisted with the devices that they are associated with. With the PLA turned off the parasitic RC's will be stored in a netlist separate from the component netlist requiring more memory space and CPU time to sort through the separate files. The use of PLA on smaller circuits is overkill and causes more work than is necessary to simulate a design.

During simulation, HSimPlus is capable of handling mixed signal designs. In order to match these mixed signals, HSimPlus uses the Newton/Raphson iteration scheme. The Newton/Raphson scheme is used to find the root of an equation. The Newton Raphson scheme provides HSimPlus with a high level of accuracy but introduces more chances for error since the equation can reach a potential answer but still be incorrect. Equation (1.1) is the Newton/Raphson equation.

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)} \tag{1.1}$$

An example of the use of the Newton/Raphson equation is found in figure 2.

$$f(x_n) = x^2 - 4$$
$$f'(x_n) = 2x$$

N	X_n	$f(X_n)$	$f'(X_n)$	X_{n+1}	dx
0	X_0=5	21	10	X_1=2.9	
1	X_1=2.9	4.41	5.8	X_2=2.14	.76
2	X_2=2.14	. 5796	4.28	X_3=2.00	.14
3	X_3=2	0	4	X_4=2.00	0

Fig. 2. Newton/Raphson Example

The first step of the Newton/Raphson scheme is to select an initial value of X plug it into the original equation and the derivative of the original equation. These values are then entered into the Newton/Raphson equation. The output of the Newton/Raphson equation is the next X value to be used in the process. The dx value represents the difference between the current and previous X values. As dx decreases the result accuracy increases. This process

is to be repeated until an acceptable result is found. The example shown resulted in a perfect answer with a final dx value of zero. Typically a value .1 or smaller is acceptable.

HSimPlus has the capability to control the precision of the parameters that it uses. The trade offs are speed and precision. The higher the precision the longer the simulation will take and the more memory it will require. There are five parameters that control the precision of major parts of the simulation. These parameters are voltage, current, small signal modeling, RC reduction, and partitioning. The main parameter to increase or decrease precision and speed is partitioning. This controls how small the blocks are that HSimPlus looks at. The range of partitioning precision is 0-4, with zero being the least precise/fastest and four being most precise/slowest. To test the time demands of the different precision ratings a simple three bit adder circuit was simulated and table I contains the results.

Table I CPU Time vs. Partitioning Precision

Precision	0	1	2	3	4
CPU Time (Seconds)	316.328	324.49	318.599	328.469	1325.426

As expected the times increased as the precision was increased, except for the precision setting of two. The two most interesting points from this test were that the processing time difference of precision four compared to three was more than four times greater, and that a precision setting of two took less time than any other precision. From this test and other simulations the best precision to time tradeoff ratio is a precision setting of two.

VI. The Effects of Transistor Number and Hierarchy on Simulation Speed

The design and simulation of an expandable circuit model was used to test HSimPlus' hierarchical netlisting. The basis for the design is a multiplier circuit which takes two 16-bit inputs, multiplies these inputs together, and outputs the resulting 32-bit number to two successive multipliers, one half of the bits to each one. This results in a cascading series of multipliers where each multiplier depends on the previously calculated solutions in order to generate the output. These chains of multiplier circuits were arranged in square patterns of 1x1 (a single multiplier), 2x2, 3x3, up to an 8x8 multiplier.

The method chosen to drive the input of the first order multipliers was a Galois Linear Feedback Shift Register (LFSR). The LSFR provides a pseudorandom, 16-bit input to the first order multipliers. Driving the cascading multipliers with the pseudorandom input from Galois LFSRs also shows what it is like to have a random data signal for input during simulations. Figure 3 below shows an example block diagram for the 2x2 multiplier circuit.

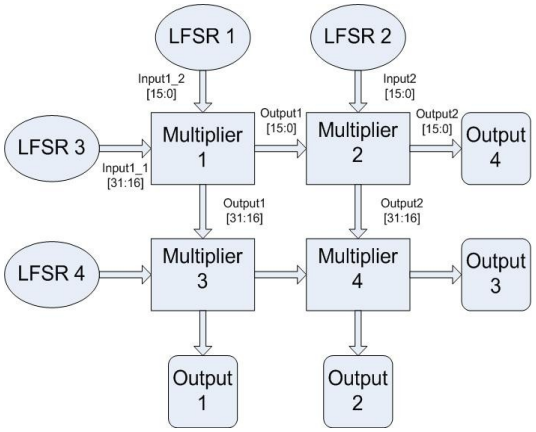

Fig. 3. Block Diagram of 2x2 Cascading Multiplier

After cascading the multiplier circuits into squares of various sizes, simulations are run to collect data on the length of CPU time it takes to simulate 40ns of circuit operating time. Using HSPICE and HSimPlus the cascaded multiplier circuits are simulated using the Micron SLP. Figure 4 below compares CPU time vs. the number of transistors in each multiplier circuit for both simulators. The point farthest left on each plot represents the time for a 1x1 multiplier, followed by the 2x2 time and so forth.

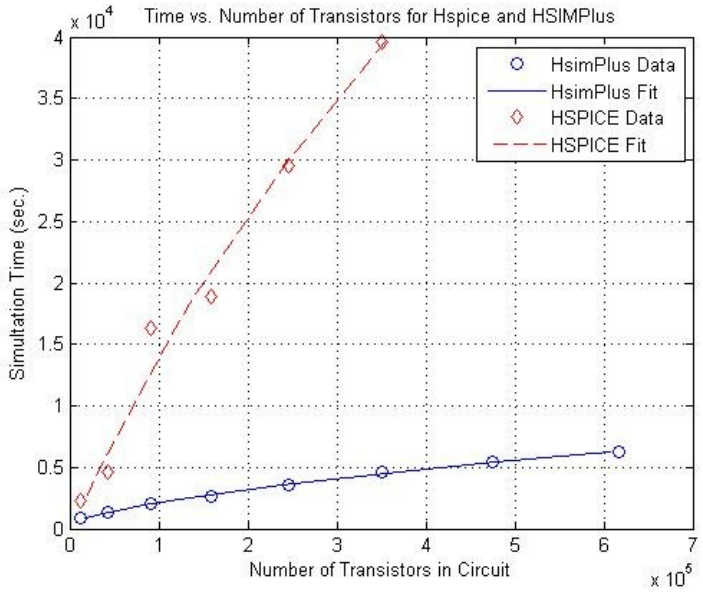

Fig. 4. Plot of CPU Time vs. the Number of Transistors

Analysis of the CPU time vs. number of transistors raises a few important conclusions. First, the CPU time for HSPICE and HSimPlus grows at a more rapid pace for the first 150,000 transistors in the circuit. However, after that point, the rate of CPU time increase becomes approximately linear with a rate of 1,000 sec./100,000 transistors for HSimPlus and 10,000 sec./100,000 transistors for HSPICE. HSimPlus exhibits this behavior because it requires a larger number of transistors in order to effectively make use of model order reduction and hierarchical analysis. The second key observation derived from figure 4 regards the difference in the amount of data points, and thus CPU times, obtained for HSPICE and HSimPlus. In figure 4 there are six HSPICE data points compared to eight HSimPlus data points. This discrepancy shows that no CPU time data was obtained for the 7x7 and 8x8 multipliers in HSPICE. This is due to the fact that the size of the HSPICE output files for the 7x7 and 8x8 are too large for the available four GB of RAM on the computers performing the simulations. Therefore, as simulation time increases HSPICE requires more computing resources in order to execute a simulation that HSimPlus can perform in a much shorter time using the same resources.

The observation with the most profound effect is the difference in the CPU simulation times. For the largest circuit HSPICE is capable of running, the 6x6 cascading multiplier, approximately 40,000 sec of simulation time was required. HSimPlus only needs about 4,650 sec to complete the same simulation. Therefore, the two-phase modeling by HSimPlus clearly exhibits a significant benefit in terms of simulation speed when compared to a standard simulation tool such as HSPICE.

VII. The Effects of Pipelining On Signal Accuracy and Propagation Delay

Due to the impedances formed by RLC networks within the PDN, power provided to circuits is inconsistently strewn with passive harmonic-like noise patterns. Equation (1.2) below shows the affects that passive elements, elements which do not generate currents or voltages, have on the voltages seen by the circuit.

$$\Delta V_{Ckt} = I_{DC} R_{PDN} + L_{PDN} \frac{dI_{AC}}{dt} \quad [2] \qquad (1.2)$$

The RLC components depicted in (1.2) directly affect the DC and AC currents drawn from the circuit sources their affect generate passive noise which in turn creates varying circuit voltages. To better illustrate the affects of (1.2) above, figure 5 and figure 6 below show a square wave clock and the affects that a simple RLC network have on it.

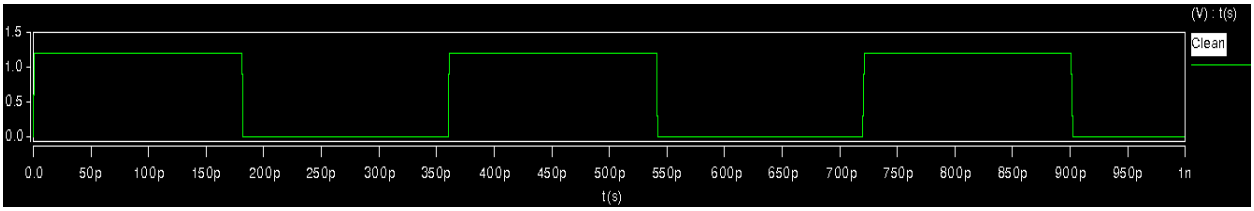

Fig. 5. Square Wave of 2.78GHz

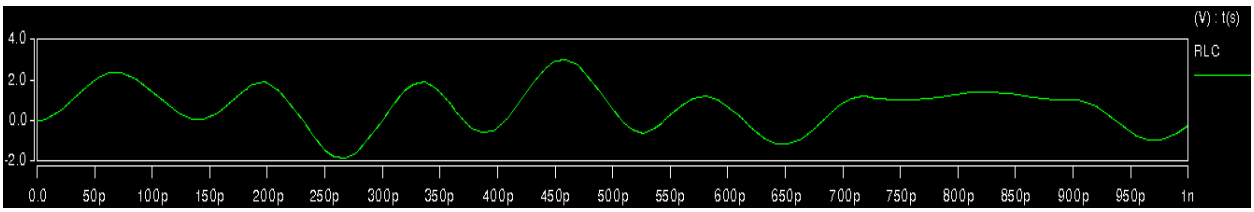

Fig. 6. RLC Network Output with a Square Wave Input

A comparison between figure 5 (a clean square wave) and figure 6 (RLC output) shows that the resulting output waveform attempts to maintain the simple square output; however, the affects of the RLC on the input signal cause the output signal to overshoot the boundaries and oscillate. Such passive noise found in the power supplied by PDNs negatively affects signals propagating through the circuit by impeding the "switch rate" at which the circuit's internal transistors actively switch. Equation (1.3) below illustrates how switching transistors are impeded as illustrated by the saturation drain current for a MOSFET transistor.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{l}(V_{GS} - V_{th})^2(1 + \lambda V_{DS})_{[4]} \quad (1.3)$$

To better understand the affects of (1.3) above it is necessary to view it together with (1.2). The passive noise introduced into the circuit voltages seen depicted by (1.2) directly affect the drain currents (I_D) of the transistors through the gate (V_G), drain (V_D) and source (V_S) voltages as seen above in (1.3). Such passive noise produces active noise through the active elements, circuit elements which independently create voltages or currents on their own, of the circuits being powered.

Multiple test circuits accurately model the affects that both passive and active noises have on a propagating signal. The test circuits comprise three main qualities: the ability to keep the active noise separate from the passive noise, the capability to know where a signal is in the circuit and when it will be there, and the means to determine whether the propagating signal should be high or low when it is observed. The first two qualities take place by designing test circuits using pipelined stages which are supplied with both clean noiseless power and noisy power produced by modeling RLC PDN affects using the Micron provided SLP. To observe the third quality, four test

circuits implementing the Fibonacci sequence were modeled and simulated starting from stage six and finishing with stages eight, eleven, fifteen and twenty three, respectfully. The signal is evaluated after each stage of the Fibonacci sequence to properly demonstrate how the noise introduced by the PDNs affects the signal's propagation delay and integrity.

The Fibonacci circuit design uses 16-bit adders in conjunction with 16-bit registers which are linearly cascaded. Figure 7 below shows a general overlay of the design of each of the four circuits.

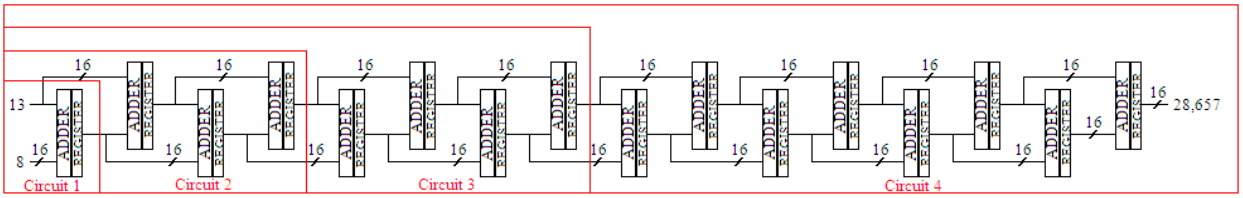

Fig. 7. Four Fibonacci Pipelined Circuit Designs

The first circuit shown in figure 7 is a single stage of the Fibonacci sequence using only one 16-bit adder and register, the second circuit advances through four stages of the sequence using a cascade of adders/registers and circuits three and four advance through eight and sixteen stages, respectfully. The circuit design is clocked to latch data on the rising edge of a 2.78GHz clock signal to properly achieve the second design quality.

Before the propagation delay is measured, a look at the power provided to the circuit better illustrates the introduction of the noise to the circuit. The voltages and currents passing through the PDN demonstrate the effects of passive and active noise on circuits power supplies. Figures 8 and 9 below show both the voltage and current sources for the test circuits.

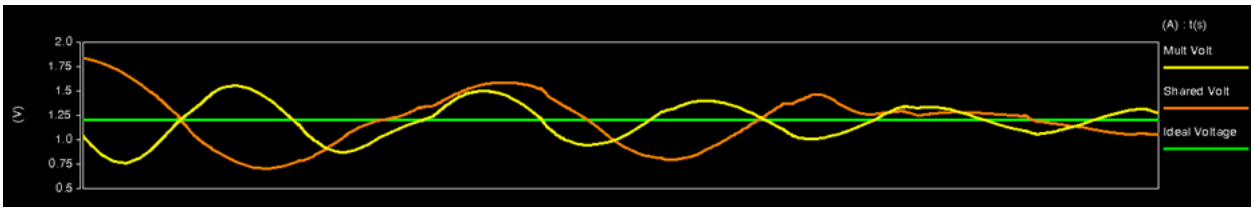

Fig. 8. Passive Voltage Noise

Both figures 8 and 9 are HSPICE simulation models of the affects on the test circuit power supplies. A closer look at figure 8 shows in green the ideal voltage that is provided to a circuit in the case where an ideal source provides a perfect 1.2V without the affects of passive noise. Note that the green line is centered at 1.2V and does not deviate in the slightest. The second line seen in orange depicts the passive noise that is introduced to the circuit

when all the circuit components are drawing their power from the same source. The passive noise introduced by a single power pack deviates from the ideal 1.2V by nearly ±.8V. The third line shown in yellow represents the passive noise that is introduced to the circuit in the event that the circuit components are being supplied by one of eight different sources. Note that the noise deviates only ±.6V when the power supply shares it's load across multiple sources.

A direct comparison between figure 8 and figure 9 shows that the passive noise seen in figure 8 directly leads to active noise shown in figure 9. Figure 9 below shows the current draw from the power supplies for the circuit.

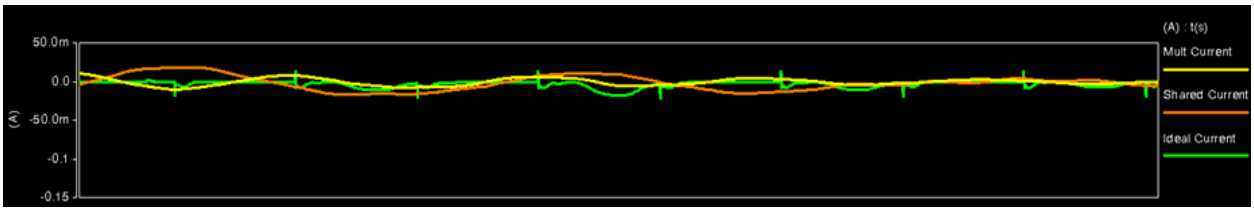

Fig. 9. Active Current Noise

It should be pointed out that the waveforms in figure 9 are color coordinated with those of figure 8, and, as such, are under the same specifications as were discussed for figure 8. With a closer look it can be seen that the passive noise deviations of the voltage source show similar deviations when compared to the currents formed by the active circuit components, these deviations oscillate and display noise patterns with the same frequency of their corresponding voltage supplies. Although the noise from figures 8 and 9 are HSPICE simulations only, the HSimplus models produce similar results where the passive and active noises shown in both the current and voltage sources oscillate at the same frequencies.

Figures 10 and 11 below show and compare the signal delays reported by both HSPICE and HSimPlus simulations. The signal delays shown are the differences between the ideal circuit model (no noise in the PDN) and the circuit models where noise is introduced via the passive circuit components of the Micron SLP model.

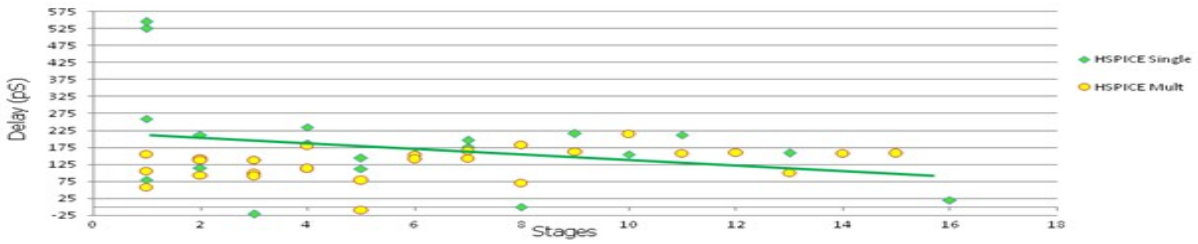

Fig. 10. Output Stages vs. Delay for HSPICE Simulations

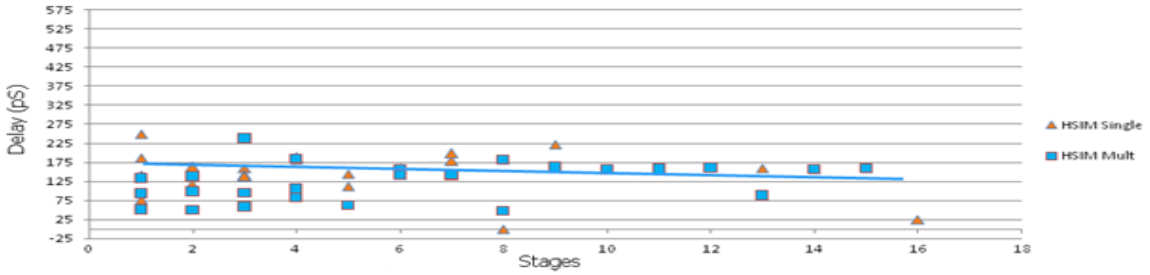

Fig. 11. Output Stages vs. Delay for HSimPlus Simulations

Observe from figures 10 and 11 that both the results from the single source simulations and those of the multiple source simulations are relatively close in the delay approximations made by the simulators. A further look into the comparisons between figures 10 and 11 show that both the HSPICE and HSimPlus data points compare against each other and are modeled in a similar fashion. A comparison of the results between HSPICE and HSimPlus shows that although close in their results, the two simulators are not perfect in their approximations. Although 70% of the results between the two simulators are within 3% of each other there are some major differences found. The biggest and worst case variance between the two simulators is seen at stage one, where a single data point from HSPICE shows a delay of 544ps, while that same data point in HSimPlus shows a delay of only 186.8ps a difference of 357.2ps. Table AI, in the appendix, gives the exact delay values for each of the data points found in figures 10 and 11 and should be referenced for point to point simulation comparisons.

There are direct correlations between the resulting power waveforms and the propagation delays found within the circuit's signals. Note that the noise from both the voltages and currents supplied to the circuit have maximum variances at the first stage of the circuit after which that variance decreases to a "steady" average value. A comparison between figures 8 and 9 (voltage and current) to figures 10 and 11 (HSPICE and HSimPlus approximated signal delays) shows that the worst case delays appear in the first stages of the circuit propagation when the noise from the power supplies is varying at its maximum. The delays then decrease to an average of 150ps (single power supply) and 130ps (multiple power supplies) as the power supplied to the circuit achieves its "steady" average voltage/current variances.

Although there exist major differences in 30% of the results produced by the two simulators, it is unclear whether those differences are due to inaccuracies produced by the HSimPlus model order reduction or whether the circuit itself is insufficient for comparing the two simulators. It is clear however, that a direct comparison can be made between the amount of noise prevalent in the power supplied to the circuit and the amount of delay a signal

will have as it propagates through the circuit. The cleaner and more consistent the power is, the more consistant the propagation delay will be.

VIII. Conclusion

The need for high-capacity, high-performance transistor-level verification has pushed today's design requirements for precise control of leakage effects to meet power budgets to its limits by demanding stable supply voltages/currents that are stable with the ever decreasing power voltages of smaller circuit technologies. HSimPlus is uniquely architected to meet the challenges of circuit verification at 65nm through its innovative hierarchical simulation, delivering the capacity needed for precise analysis of post-layout effects. The hierarchal simulation capabilities were tested through experiments on cascaded multiplier circuits. For every 100,000 transistors added to the simulation, HSPICE requires ten times the CPU time of HSimPlus. In addition, HSPICE was unable to finish the simulations on the 7x7 and 8x8 multipliers due to the fact that it utilizes a much greater amount of system resources available on the simulating machine.

With the addition of parasitic impedance networks introduced through the PDNs, delays were also introduced to the propagating signals. To properly measure the amount of delay for the propagating signals a series of cascading adders was used to systematically observe signal integrity throughout the circuit. A worst case delay of 544ps was measured at stage one which can be directly correlated to the worst case power noise fluctuations seen at the same stage. With a few exceptions, HSimPlus' simulations were within 3% of the same simulations done by HSPICE. Although there existed major differences in 30% of the results produced by the two simulators, it is unclear whether those differences are due to inaccuracies produced by the HSimPlus model order reduction or whether the circuit itself is insufficient for comparing the two simulators. It is clear, however, that a direct comparison can be made between the amount of noise prevalent in the power supplied to the circuit and the amount of delay variation a signal will have as it propagates through the circuit. The cleaner and more consistent the power is, the more consistent the propagation delay will be.

APPENDIX

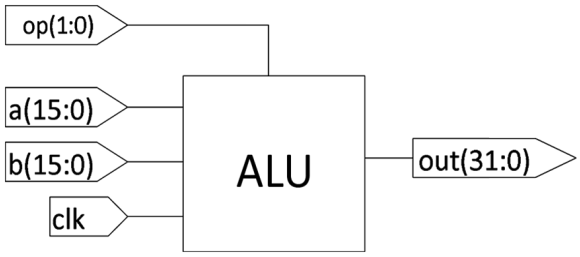

Fig. A1. One ALU Circuit

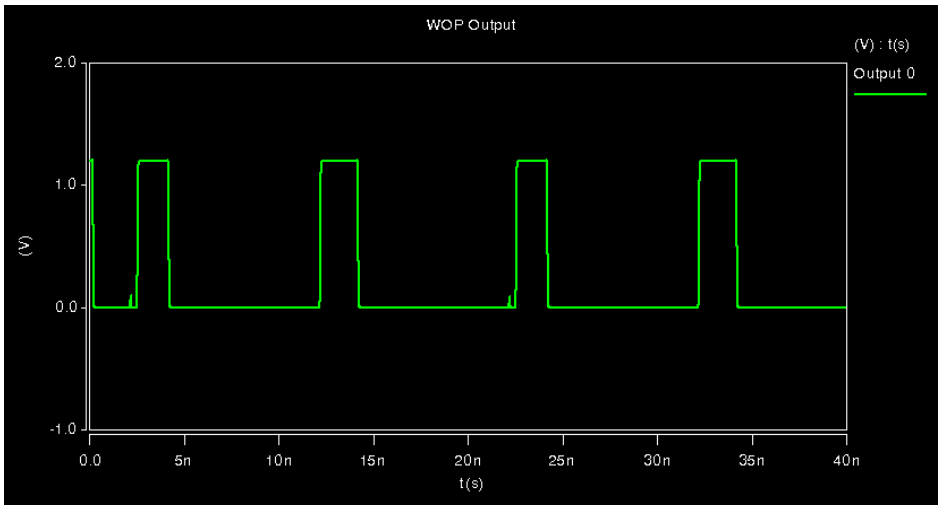

Fig. A2. WOP Square Wave Output

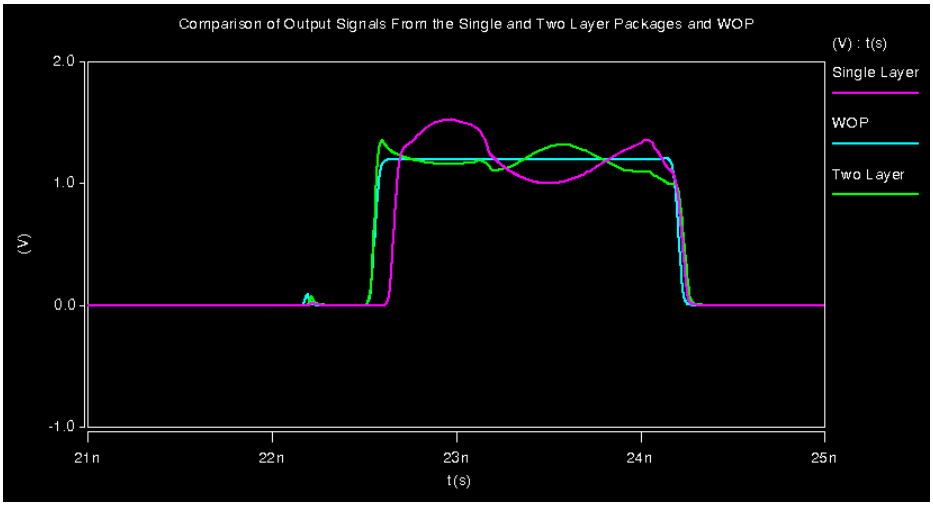

Fig. A3. Three Output Signals of One Layer, Two Layer, and WOP in HSPICE

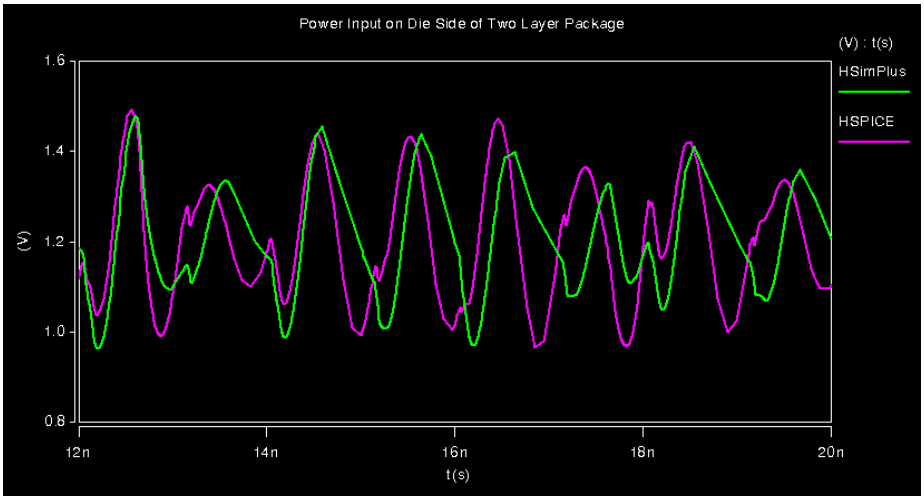

Fig. A4. Phase Difference, Power Output HSimPlus vs. HSPICE

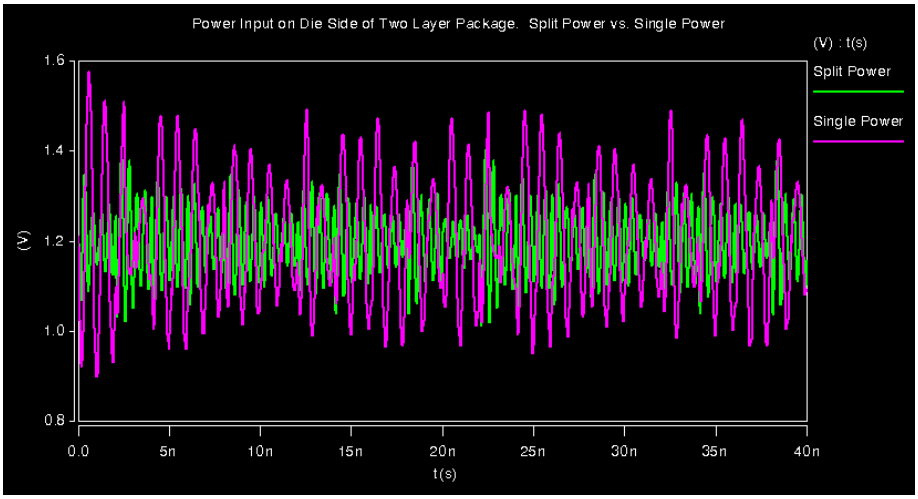

Fig. A5. Power Input on Die Side of Two Layer Package, Split Power vs. Single Power

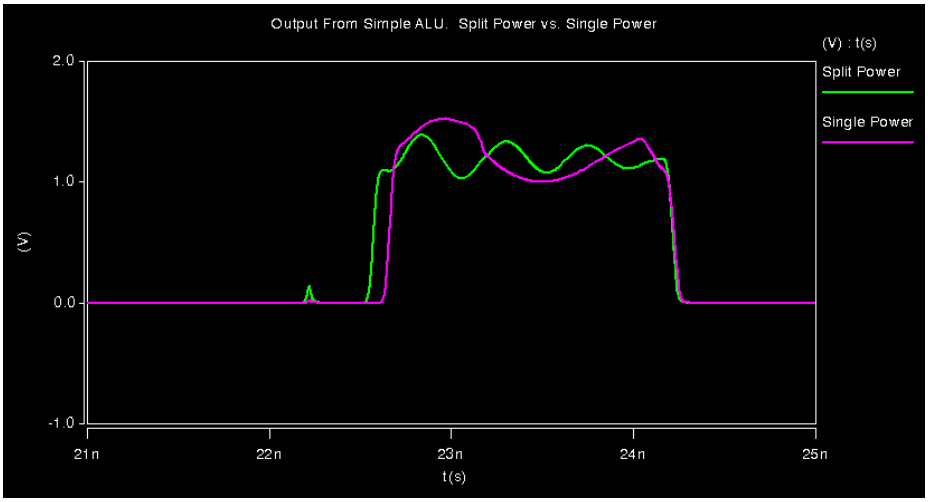

Fig. A6. Output Signal, Split Power vs. Single Power

Table AI Signal Propagation Delay Based by the "Golden" Model without Noise

Stages	HSPICE Single (ps)	HSPICE Multiple (ps)	HSimPlus Single (ps)	HSimPlus Multiple (ps)
1	79.83	56.8	77.44	50.2
1	259.4	104.8	142.4	93.2
1	524.8	153.8	249.8	132.8
1	544.8		186.8	
2	212	141	163	98
2	114	92	115	50
2	137	137	138	138
3	-22	98	159	94
3	139	90	140	58
3	137	137	138	238
4	183	112	181	83
4	234	113	188	105
4	186	179	185	184
5	111	-11	112	-33
5	143	78	144	62
6	157	151	158	157
6	140	140	141	141
7	177	164	178	140
7	195	142	198	143
8	0	70	0	47
8	182	181	182	182
9	215	162	221	163
10	154	214	155	155
11	211	157	158	158
12	159	159	160	160
13	158	99	159	88
14	156	156	157	157
15	158	158	159	159
16	19		25	

REFERENCES

[1] D. Blaauw, R. Panda, and R. Chaudhry, "Design and analysis of power distribution networks," in *Design of High-Performance Microprocessor Circuits*, A. Chandrakasan, W. J. Bowhill, and F. Fox, Eds. Piscataway, NJ: IEEE, 2001, pp. 499-522.

[2] Synopsis Reference Manual (2009.

[3] Tim Hollis, "University of Utah Senior Clinic 2009-2010". [PowerPoint Presentation]. April 10, 2009.

[4] A. S. Sedra and K.C. Smith (2004). Microelectronic circuits (Fifth Edition ed.). New York: Oxford. p. 552.

ETHICAL AND SOCIAL ISSUES

"1. What are the ethical issues that you encountered during completion of the project? How did you tackle them? You should discuss the issues that you needed to consider while making decisions about the project as well as issues that might affect users and non-users of the system after implementing the project. (Just to give you one example, engineering designs almost always involve compromises between cost, performance capabilities, and possibly adverse consequences. The choices you make should include considerations of ethics in addition to technical and economical issues.)"

In order to use the IBM 65nm package libraries we had to sign a non-disclosure agreement (NDA). We wanted to use the libraries but this would prevent us from putting our entire testing method out into the open. If we were to publish this information out into the open, we might have an injunction placed against us, be sued, and have criminal charges pressed against us. These trade secrets are illegal to share under the Economic Espionage act of 1996. If we were to let this information be leaked, through no fault of our own, then it is possible that we might be blamed and be forced to face the consequences (jail time). This of course would deprive us of the ability to feed our families. This in turn would force our spouses to turn to professions of questionable morality in order to support our families. This train of thought opens up an entirely different Pandora's Box, so I will stop here. The other question we had was what was a sufficient level of accuracy necessary, to achieve to conclude that HSimPlus was accurate enough? We eventually decided that a sufficient level of accuracy is any level of accuracy that will result in a working circuit.

"2. Explain what potential impact (assuming that you were able to accomplish all your goals) your project has to society as a whole. Do not just include the improved technical capabilities of your system. Will it have any effect on the quality of life? Are there any environmental effects (positive or negative) that one must be aware of while planning to manufacture the product? Think of multiple questions such as these while developing your report."

The verification and use of the two phase model in power delivery network analysis makes the creation of much larger circuits possible. For example the NVIDIA GeForce GTX 480 GPU has 3 billion transistors. Any simulation using HSPICE would take an inordinate amount of time and would make it very difficult to design or verify such a large circuit. These large circuits can have a negative effect on the quality of life. These advanced CPUs and GPUs can be used create immersive graphical worlds. These worlds have been shown to be extremely addictive. People who play these MMORPGs generally gain weight, have lower grades, and have a diminished real world social life.

Additionally, the additional power requirements for running these millions of computers create a drain on our national power resources, and contribute to global warming. They can also have a large positive effect on the quality of life, enabling researchers to map the human genome, and to come up with new and innovative drugs to combat disease.