Design-for-Test and Calibration for Silicon Photonics using Ring Resonators and Wavelength Division Multiplexing

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***Abstract*—Advances in silicon photonics (SiP) are enabling large-scale integration and deployment of photonic integrated circuits. SiP is susceptible to manufacturing variations which necessitates efficient techniques for their testing, validation, and tuning. We propose a novel design-for-test and calibration (DFTC) solution based on a wavelength division multiplexing scheme, where the operating wavelength is multiplexed with test signals on the same waveguides, enabling online testing. The architecture employs ring resonators as wavelength-tuned filtering devices to test signals at judiciously chosen test points to compare against a reference for fault detection. Moreover, if deviation of design performance is detected, our DFTC circuit enables tuning and calibration to bring performance within acceptable margins. We describe the DFTC circuit design and present simulation results that demonstrate its efficacy.**

***Index Terms*—design-for-test, calibration, silicon photonics, manufacturing variation, ring resonator, wavelength division multiplexing.**

I. Introduction

Recent advances in *Silicon Photonics* (SiP) technology are enabling large-scale integration of hybrid opto-electronic or photonic integrated circuits (PICs). Nowadays, a variety of devices – such as optical switches, transceivers, modulators, detectors, etc. – are being integrated with conventional (bulk/SOI) CMOS electronics using 300mm diameter wafers and existing 45nm CMOS (or higher) fab facilities. This is resulting in larger scale integration and manufacturing cost reduction [1]. In addition to high-speed, high-bandwidth, low-power on-chip communications, SiP is also being utilized as switching and computing fabrics. Altogether, this is bringing *a convergence of communication and computation on a unified platform* while advancing a wide range of applications such as artificial intelligence (AI) and machine learning (ML) with optical neural networks [2], optical logic, quantum/reversible computation [3], etc.

This increase in on-chip integration density is, however, posing a significant *challenge of testing and calibration of PICs.* SiP device operation is sensitive to variations in the manufacturing process [4][5]. Imperfections in lithography processes lead to variations in device geometry and layout. This may shift a device's response off its design parameters, resulting in not just performance degradation but also system failure in the worst case. Moreover, limited advances in photonic design automation has rendered much of PIC design as semi-custom. This raises the potential for design errors or faulty design margins. Therefore, PICs need to be tested for normal operation before deployment. In addition to testing for fabrication defects, PICs are also required to undergo *calibration (or tuning)* [6] so as to bring their performance within the tolerance limits of the specifications.

Despite a few PIC testing automation [7] and calibration efforts [8], this process is manual and tedious, lacks the required automation, and incurs a high cost. Therefore, the development of **design-for-test and calibration architectures and circuitry in the photonic domain**, along with techniques for insertion of test-access points, and CAD tools for automatic test pattern generation (ATPG) is becoming an imperative. To quote from the 2021 Hybrid Integration Roadmap's chapter on Test for Photonic Devices [9]: *"Design-for-Test (DFT) including optical test access points, Built-in-Self-Test (BIST), redundancy for self-repair and prognostics to report changes and deterioration over the life-cycle of optical products are desirable and of value in an increasing number of applications. These should be considered for inclusion not only in designs but in software design tools as well."*

Contributions: To address the above needs and challenges, this paper presents a novel design-for-test and calibration (DFTC) architecture to test silicon PICs. The DFTC circuit blocks are specially designed photonic circuits that are inserted at a set of judiciously chosen nets/waveguides in a design under test (DUT). The DFTC circuits are inactive during the normal operation of the chip, and are enabled only in test mode. They are designed to capture test signal power under the application of specific test input patterns, and to

compare it against the expected response (reference laser). The objective of our DFTC approach is to detect malfunction due to fabrication defects or manufacturability variations, and to enable/simplify DUT's tuning and calibration, if applicable.

Our DFTC architecture is based on SiP ring-resonators (RRs) [10], which are used as wavelength filters and modulators to inject and filter out optical test signals. These are designed to introduce minimal design overheads, such as low insertion loss and area overheads. The architecture allows multiplexing of multiple test points to reduce test IO pins. An enhancement to the basic DFTC architecture is also presented that allows the use of test signals of different wavelengths than the normal (operating mode) wavelength. Using RRs and wavelength division multiplexing (WDM) allows *on-line test* of the DUT, without disconnecting it from the system.

We demonstrate the application of our DFTC approach on a practical photonic benchmark design – an optical neural network PIC which was fabricated and whose function was demonstrated in [2]. The DFTC circuits are designed and simulated using the LUMERICAL suite of tools [11]. They are inserted in the benchmark design and defects are detected by applying test patterns and test-signal capture. Note that the full potential of our DFTC approach would require the development of CAD tools for identification of suitable test-points and a corresponding ATPG tool. However, algorithms for SiP test-point selection and ATPG are beyond the scope of this paper, and a subject of on-going research.

Paper Organization: The following section reviews previous work and limitations. Section III covers background concepts. Section IV first provides an overview of our DFTC architecture and methodology, and then describes the details of the DTFC components. Section V shows how the DFTC architecture can be augmented to perform on-line test. The results of RR design and simulation are provided, highlighting their usage as low-loss, wavelength selective WDM filters. Section VI demonstrates the application of DFTC insertion and test on a photonic design benchmark. Section VII concludes the paper.

II. PREVIOUS WORK

A test station for semi-automatic wafer-level characterization of silicon photonics devices has been proposed in [7]. Several features such as fiber alignment, insertion loss etc. have been incorporated that are aimed at optimizing the accuracy and reproducibility of the measurement results. Similar developments for die and wafer level testing and probe access have been presented in [12] [13], using varied fiber coupling techniques. On the other hand, specific techniques for on-chip phase monitoring [14] or post-fabrication trimming [15] have been presented for testing and calibration of PICs. The utility of such test infrastructure would be greatly enhanced with the development of compatible SiP DFT architectures.

While performance degradation of PICs under manufacturing variations is well-known, there have been few attempts to develop defect and failure models [16] and analysis techniques to quantitatively estimate their impact on PIC's performance [17]. In the absence of such models, SiP DFT techniques would further assist in test and yield improvement.

The recent work of [18] introduces a DFT solution to test SiP circuits. They propose the use of a Mach-Zehnder Modulator (MZM) as a device to capture test signals, and the use of a passive Y-combiner to compare the captured signal against a reference. However, a significant drawback of their approach is the very high insertion loss due to DFT insertion – their experiment shows 2.6dB insertion loss per test access point. This makes it impractical to insert multiple test-access points. Their test-access MZI is also very large ($> 5\mu m$ length), which also introduces large area overhead. In contrast, the proposed DFTC architecture is low loss, enables multiple test point insertions, and allows on-line test via WDM.

III. BACKGROUND

In this work, we assume that the PIC under test comprises the following passive and active devices: fundamental mode SOI waveguides (straight waveguides, bends, crossings), Y-splitters and combiners, waveguide couplers, electro-optic or thermo-optic phase modulators (PMs), Mach-Zehnder Interferometers (MZIs), Ge photodetectors, absorbers, etc. Fig. 1 (a) depicts the waveguide profile and dimensions that we have used for the designs and experiments conducted for this paper. Figs. 1 (b) and (c) depict the active devices used in the DUT. Our DFTC architecture does not preclude the use of resonance cavity structures in the DUT; however, in our experiments, we use RRs only in the DFTC circuits, but not in the DUTs.

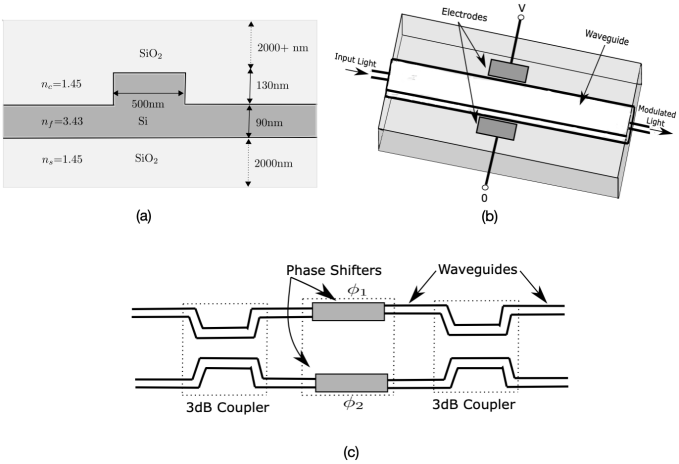
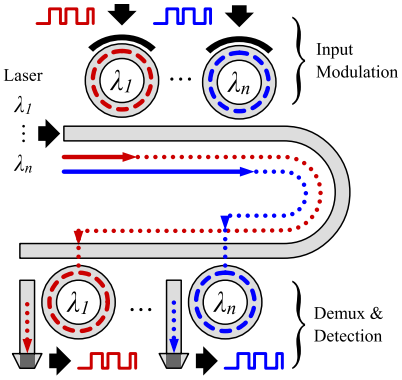


Fig. 1: SiP devices used in the DUT PICs: (a) SOI waveguide profile and the dimensions used; $n_f = 3.43$ is the refractive index of Si, $n_s, n_c = 1.45$ that of SiO_2; (b) phase modulator; (c) 2×2 MZI.

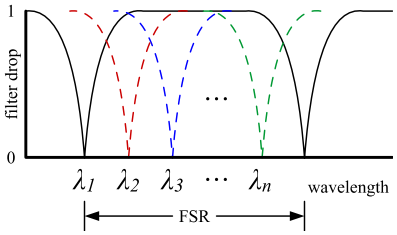
A. RRs and WDM

A key component of our DFTC architecture is the RR. It is used as a sensitive wavelength filtering device. It is used to couple in to a waveguide (or filter out from it) a signal of wavelength λ_0, which is the resonant wavelength of the ring. Because of its high wavelength selectivity, it is used in WDM architectures, as shown in Figs. 2a-2b.

In a WDM system, channels of data are assigned to specific wavelengths of light. RRs tuned to specific resonant wavelengths are used to modulate this light and inject signals into the waveguide. Light is routed through the communication and computation fabric. At the receiving end, RRs are used again as demultiplexers to filter out particular wavelengths.



(a) Modulation (MUX/DeMUX) using RRs



(b) WDM: Channel wavelengths within the FSR of a RR

Fig. 2: WDM system with RRs: An overview

The filtering response of a RR is periodic w.r.t. wavelength. The wavelength range between consecutive filter peaks is called the Free Spectral Range (FSR). A number of channels can be packed within the FSR, and the spacing between them can be very small (a few nm). This is shown in Fig. 2b.

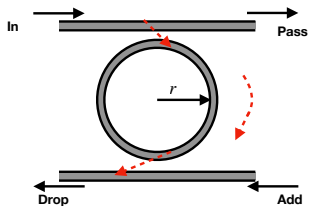


Fig. 3: Add-Drop RR.

In our DFTC architecture, we use RRs as Add-Drop RRs as shown in Fig. 3. At resonance, a signal (λ_0) is coupled through the "In" port, travels the half circumference, and is coupled out of the "Drop" port. Let r be the radius of the ring waveguide, and circumference $L = 2\pi r$, and $\beta = 2\pi n_{eff}/\lambda_0$ be the propagation constant. Here n_{eff} is the effective refractive index of the ring. The ring is in resonance when the round trip phase in the ring is an integral multiple of 2π:

$$\phi = \beta L = \frac{2\pi n_{eff}}{\lambda_0} L = 2\pi m \tag{1}$$

Eqn. (1) gives a relationship that defines the radius of the ring. Moreover, the FSR of the ring is given as $FSR = \frac{\lambda_0^2}{n_g L}$, where n_g is the dispersion dependent group index of the waveguide. Two other measures are associated with the sharpness of the resonances: *Finesse* and the *Q-factor*. Let FWHM denote the full width at half maximum of the resonance spectrum. Then:

$$Finesse = \frac{FSR}{FWHM}; \quad Q\text{-}Factor = \frac{\lambda_0}{FWHM}. \tag{2}$$

Finesse describes the sharpness of resonances relative to their spacing, and the Q-factor describes the sharpness of the resonance relative to its central frequency. We use the above quantities to demonstrate the efficacy and application of our RR based DFTC architecture.

IV. DFTC Architecture Overview

Fig. 4 depicts a high-level block diagram of the DFTC architecture. The architecture partitions the DUT into n subcircuits around which test-points are inserted (denoted Block $1, \ldots,$ Block n). These test points allow to localize critical signals for easy probing and measurements. In each DFTC block, the subcircuit under test (SUT) is preceded by a *Test Insertion Point* – a photonic circuit that injects (or couples) optical/laser test signals into the input waveguide. At the output of the SUT a *Test Access Point* is inserted, where the test response output of the SUT is captured and sent to an optical comparator circuit. Our DFTC also contains an *optional Calibration point* – comprising an electro-optic phase modulator and/or a Germanium (Ge) absorber. The calibration point can be placed at the output of the SUT's waveguides to adjust the phase using the phase modulator, or attenuate the signal using a Ge absorber, if needed. Optical test signals can be injected into different DFTC blocks using an optical demultiplexer (DeMUX), and they can be filtered out from different blocks through an optical MUX and sent to one optical comparator circuit.

As for comparison of the test response signal against the reference, we re-use the strategy of [18]: A *Y-combiner* is used to combine the test response and reference. The reference

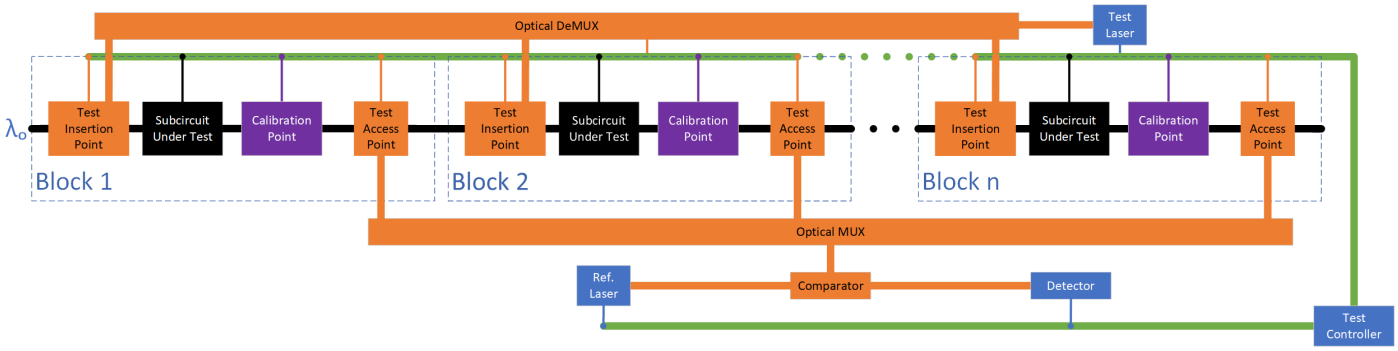


Fig. 4: SiP DFT and Calibration Architecture: Overview

signal power corresponds to the (ideal) fault-free response at the test access point, which can be computed by an ATPG tool by analyzing the circuit layout, propagation constants and loss parameters. The reference signal is phase shifted from the ideal (fault-free) response by π radians – i.e. the reference signal is of opposite phase than the fault-free signal. The output of the Y-combiner is measured using a Ge photodetector. If the output is zero, the SUT is defect-free as it implies that the test and (π-phase-shifted) reference signals *destructively* interfere and cancel out. Otherwise, the SUT is defected.

The DFT architecture also comprises a *Test Controller* that activates test access points and test signal capture, and allows multiplexing of multiple test-access points onto one set of test pins. It uses electrical controls to activate different DFTC blocks by modulating (switching ON or OFF) the MUX/DeMUX and the test insertion and activation points.

A. Design Details with Ring Resonators

Fig. 5 depicts how ring resonators are used as resonance based devices to inject and extract test signals in each DFTC block. The subcircuit under test is designed for a specific operating wavelength λ_0. The test laser also produces a test signal of the same wavelength λ_0. The *DeMUX* comprises of n RRs that are (statically) tuned to the resonance frequency λ_0. Each RR is also designed with a phase modulator (a P-i-N diode around the ring waveguide) such that application of voltage causes carrier injection or extraction and changes the effective index of the ring. This effectively *detunes the ring off-resonance* at λ_0. Thus, to test Block i, only the i^{th} RR in the DeMUX is in resonance, and others are detuned.

Similarly, the RRs at the DFTC Add and Drop Ports are also tuned for resonance at λ_0. These are activated to inject the test signal into the SUT, and also capture the response by filtering it out of the Drop Port. Finally, the *optical MUX* also comprises n RRs, and operates inversely to the DeMUX, routing the signal to the comparator. The test controller is responsible for tuning and detuning the corresponding RRs. Under normal mode, all RRs are tuned off-resonance at λ_0.

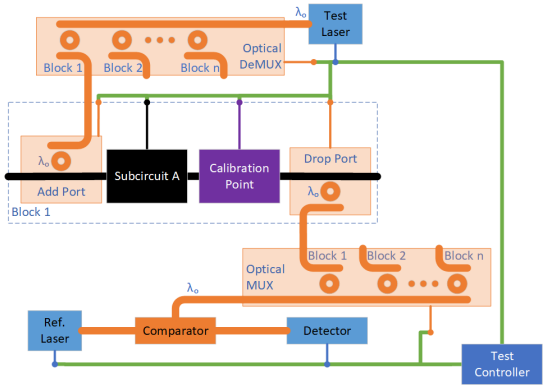


Fig. 5: Details of a DFTC block with RRs

V. Online Test: Multiple Test Signals and WDM

Figure 6 describes an enhanced configuration of the DFTC architecture, where the test signals are wavelength-division multiplexed using ring resonators. The architecture uses two test signals λ_- and λ_+, which are of different wavelengths than the normal mode (operating) wavelength λ_0. The benefit of using separate test signals (λ_-, λ_+) is that they do not interfere with λ_0, and this allows the testing to be performed automatically without taking the PIC off-line in the field.

The test signals are chosen in such a way that $\lambda_- < \lambda_0 < \lambda_+$, and that $\lambda_0 = (\lambda_+ + \lambda_-)/2$. To accommodate the two test-signal wavelengths, the DFTC blocks — DeMUX, MUX, Test Insertion (Add) Port, Test Access (Drop) Port — require 2 RRs, each tuned to λ_- and λ_+ resonant wavelengths. The RRs are designed to have a sufficiently large FSR and their response is selective only to the target wavelengths, so that the test signals are selectively filtered out and probed.

With the design of Fig. 6, our objective is to detect faults/defects in the PIC under normal mode wavelength (λ_0), but by observing their response to the two test wavelengths (λ_-, λ_+). In other words, we extrapolate the normal mode response $R(\lambda_0) \approx (R(\lambda_-) + R(\lambda_+))/2$. This is a workable approximation, as the DUT comprises mostly of *linear optical*

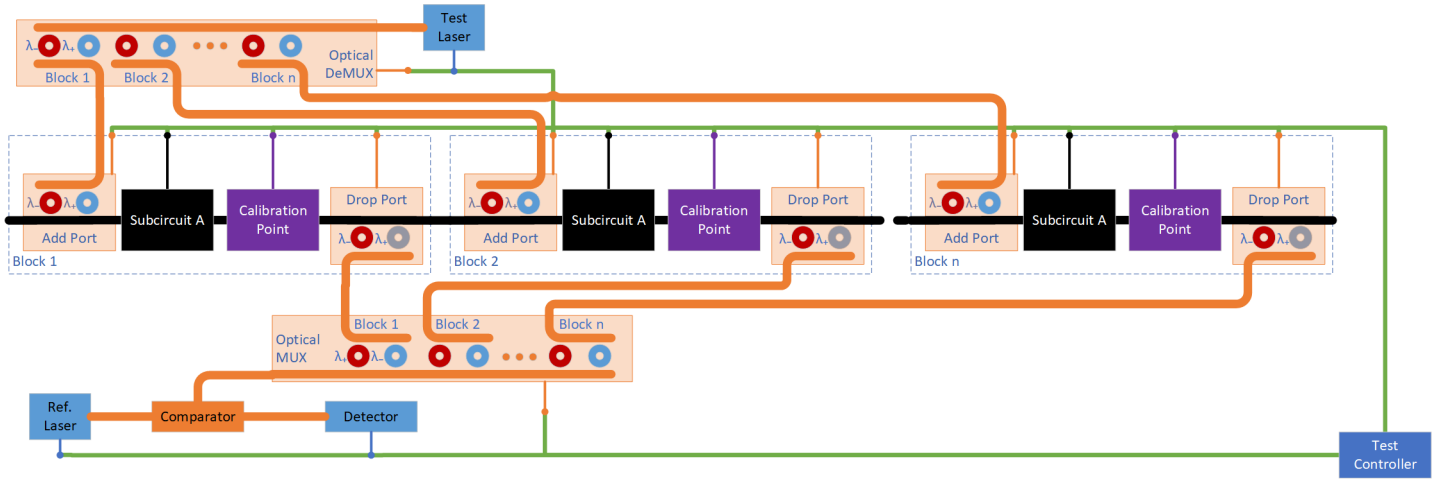


Fig. 6: DFTC Architecture details: Use of ring-resonators as test insertion and access points, use of separate normal mode (λ_0) and test-mode wavelengths (λ_-, λ_+), and a test controller to apply test inputs to compare DUT signals against a reference.

devices. The rationale for using two test wavelengths spaced equally apart from λ_0 is to extrapolate the expected response in such a way that the approximation errors cancel out and the presence of defects can be robustly established.

Design data: We have designed 3 different RRs each tuned to a different resonant wavelength $\lambda_-, \lambda_0, \lambda_+$, respectively. We choose $\lambda_0 = 1550nm$, which is a popular wavelength of choice for SiP; and the test wavelengths $\lambda_- = 1540nm, \lambda_+ = 1560nm$. Each RR is designed with the FSR = 15nm, so that none of the RRs select each other's wavelengths. RRs were designed and simulated using the LUMERICAL photonics suite [11]. Table I presents the design and simulation results. The results show that the RRs have low insertion losses, a fairly compact size, and other figures of merit that are within a normal range of SiP RRs.

TABLE I: Design Data for three RRs tuned for different resonant wavelengths. FSR of each RR is fixed at 15nm.

RR Design Data	$\lambda_- = 1540nm$	$\lambda_0 = 1550nm$	$\lambda_+ = 1560nm$
Circumference	43.61μm	44.15 μm	44.70μm
Q-factor	5407	6447.15	6406
Finesse	52	62	61.6
Extinction ratio	32.67dB	32.55dB	32.60dB
Insertion Loss	0.138dB	0.25dB	0.20dB

The ring with resonance at λ_0 is used in the DFTC architecture of Fig. 5, but is not required in the set up of Fig. 6. Fig. 7 shows the transmission response of each ring, depicting the FSR of 15nm, and that none of the rings pick up the other wavelengths.

VI. DEMONSTRATION ON A BENCHMARK DESIGN

Consider the optical interference unit of a silicon photonic neural network chip [2] comprising couplers, MZIs and phase modulators, as shown in Fig. 8. The MZI's and waveguide

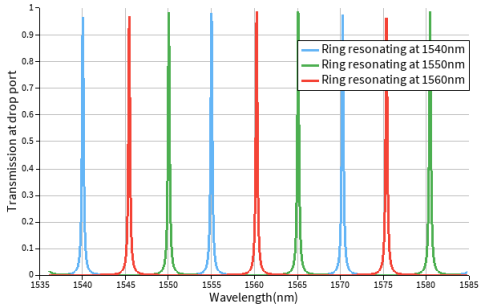


Fig. 7: Transmission response of $RR(\lambda_-)$, $RR(\lambda_0)$, $RR(\lambda_+)$.

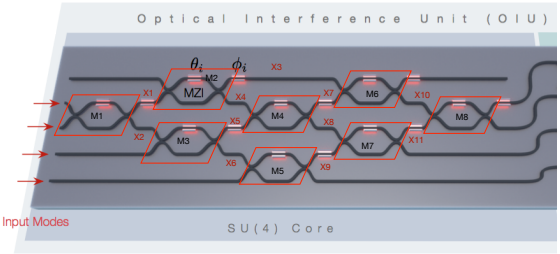


Fig. 8: SiP neural network subcircuit, borrowed from [2]. The MZIs are annotated $\{M_1, \ldots, M_8\}$ and the internal waveguides as $\{X_1 \ldots, X_{11}\}$.

interconnects are annotated as $\{M_1, \ldots, M_8\}$ and $\{X_1, \ldots, X_{11}\}$, respectively. We have modeled this subcircuit in Lumerical, where the individual devices (MZIs, PMs) were designed using FDTD and CHARGE solvers and their *S*-parameters were exported to the INTERCONNECT tool to model this circuit. All devices were designed for wavelength λ_0. Each MZI operates in a *bar configuration* when 0V is applied to its control arm, in a *cross configuration* for 7.5V, and in an intermediate configuration between 0V and 7.5V.

We choose the waveguide $X7$ (top output arm of MZI M_4) as the test access point and insert the WDM-based DFTC block. We introduce defects at the MZI M_3 and demonstrate that the faulty and fault-free values can be distinguished by capturing the responses at X_7. Suppose that under the fault-free case, the MZI configurations are: $M_1 = cross$, $M_3 = bar$, *and* $M_4 = cross$. All three wavelengths are injected at the top arm of M_1, traversing $X_2 \rightarrow X_5 \rightarrow X_7$. Defects in M_3 are simulated by configuring it in intermediate states by applying control voltages of 1V, 2V and 3V. In this way, M_3 is not in a complete bar configuration and some power crosses over into both arms. For our experiments, all three wavelengths $\lambda_-, \lambda_0, \lambda_+$ are injected into the PIC, and the signals are filtered out at X_7 via the 3 RRs. We measure the transmission power at the drop port of the RR. Results are shown in Table II.

TABLE II: Transmission measured at RR drop port at X_7. Defects simulated in M_3.

MZI Configurations	Trans. for λ_-	Trans. for λ_0	Trans. for λ_+	Average Trans. $(\lambda_- + \lambda_+)/2$
Defect-free	0.870	0.842	0.853	0.862
Defect (1V)	0.783	0.701	0.823	0.803
Defect (2V)	0.598	0.491	0.626	0.612
Defect (3V)	0.377	0.312	0.407	0.392

Results show that for the defect-free condition, the average response of the test-mode wavelenghts is similar to that of the normal (operating) mode λ_0. In presence of defect, the average transmission of test wavelengths is different than λ_0. The test wavelengths and normal mode wavelength experience different phase change with the application of voltage. This leads to distinct power distribution at X_5 and X_8 with each wavelength. This further leads to nonidentical transmitted power at X_7 in presence of defects, distinguishing the defect-free PIC from the defected one. The experiment demonstrates the application of our DFTC strategy to detect malfunction, and highlights the promise of our WDM-based test approach.

VII. Conclusion and Future Work

This paper has presented a design for test and calibration architecture to detect malfunction in a silicon PIC. Our architecture injects test signals in a DUT, and also captures its response using ring resonators as wavelength filtering devices. The DFTC architecture can also be deployed for online test, using a wavelength division multiplexing approach. We have demonstrated ring resonator designs that can be used robustly to selectively inject and filter out test signals at test insertion and test access points. We have also demonstrated the application to test measurements of our DFTC architecture on a optical neural network subcircuit and shown how it can help in detecting defects. As part of future work, we are continuing to expand upon our experiments and also investigating algorithms to generate test patterns for PIC testing.

VIII. Acknowledgment

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