# Silicon Photonic Test-Point Selection by Integrating Design Parameters with Hypergraph Partitioning

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***Abstract*—As silicon photonic integrated circuits (PICs) increase in complexity, ensuring their reliability against manufacturing and operational variations necessitates robust Design-for-Test (DfT) strategies. We present an adaptable methodology for DfT insertion in large-scale PICs, centered on physics-informed hypergraph partitioning. Our approach uniquely leverages hypergraph-based weighting derived from process sensitivities (e.g. etch, doping) and operational drifts (e.g. thermal, injection), quantified using partial derivatives from foundry data or Transfer Matrix Method (TMM) simulations. This assigns actionable risk values to both devices (nodes) and interconnects (hyperedges). We employ k-way partitioning to achieve finer sub-network isolation and targeted test access, crucial for vulnerability localization in complex PICs like multi-level ring resonator networks or large MZI-based crossbars. Experiments performed on PIC designs demonstrate the application of the proposed risk coverage metric to vulnerability localization and test point insertion, achieved with quantifiable and moderate overhead.**

## I. Introduction

Silicon photonics is revolutionizing high-bandwidth, low-power integrated circuits for demanding applications in data centers, machine learning, computing, and sensing [1]. However, as Photonic Integrated Circuits (PICs) grow in complexity, integrating numerous ring resonators (RRs) [2], Mach–Zehnder interferometers (MZIs) [3], and multi-mode interferometers (MMIs), their susceptibility to manufacturing variations (e.g., in lithography, etching, doping [4]) and operational drifts (e.g., thermal fluctuations [5]) becomes a major challenge. Ensuring reliable performance and acceptable yield necessitates robust testing and Design-for-Test (DfT) methodologies tailored to the unique characteristics of photonic devices [6].

The area of testing of silicon PICs is beginning to witness increasing research and developmental efforts — not only the development of probe stations and monitors for die- and wafer-level test [7] [8] [9], but also the design of novel silicon photonic DfT architectures [10] [11] to enhance controllability and observability, and simplify calibration/tuning. However, contemporary photonic DfT approaches lack the requisite test automation techniques and tools to: 1) judiciously select devices or waveguides in a PIC as test/debug points for DfT insertion; and 2) perform automatic test pattern generation (ATPG) to drive critical functions of the PIC for testing. Resultingly, they lack the granularity to localize failure-prone components or regions within complex PICs.

*Contributions:* To address this gap, this paper proposes a novel *physics-informed test-point selection or DfT insertion methodology*, specifically designed for large-scale silicon photonics. Our core contribution is a *hypergraph-based risk weighting heuristic* that assigns quantitative risk metrics to both photonic devices (nodes) and their interconnecting waveguides (hyperedges). These weights are derived from the components' sensitivity to critical fabrication mismatch parameters (e.g., geometry deviations, doping non-uniformity, thermal sensitivity), with sensitivity coefficients ($\kappa$) obtained from foundry process data or detailed Transfer Matrix Method (TMM) simulations [12].

We employ advanced hypergraph partitioning techniques to systematically identify and isolate high-risk sub-networks within the PIC. We utilize *k-way partitioning*, implemented via the **KaHyPar** tool [13], constrained by a balance factor ($\epsilon$) to ensure meaningful divisions. This approach enables finer vulnerability localization and more targeted placement of DfT resources – such as test-signal injection couplers, photodiodes, monitors, response-signal capture taps, etc.

The paper details the complete flow: (1) vulnerability or risk assessment of devices/waveguides via partial derivatives of their optical response to process or thermal parameters, (2) hypergraph-based weighting and normalization, (3) multi-way partitioning under explicit balance constraints, and (4) identification of test insertion points for placement of DfT structures for easy probing and measurements. The approach is programmed as a CAD tool, and its application is demonstrated on three different PIC benchmarks. The result is a scalable DfT insertion and test-point selection methodology that captures both device- and interconnect-level sensitivities in modern silicon PICs. [14].

*Paper Organization:* The following Section reviews related previous work and puts this work in perspective. Section III identifies key fabrication mismatch parameters that are modeled in our heuristics. Section IV describes how these mismatch parameters are used as weights in the hypergraph model. Section V describes how sensitivity coefficients are derived from transfer matrices. Section VI describes our partitioning strategy and test point selection. Section VII describes our implementation and Section VIII describes experimental results. Section IX concludes the paper.

## II. Previous Work in PIC Test & DfT

While performance degradation of PICs under manufacturing variations is well-known [15], there have been few attempts to develop defect and failure models [16] and analysis techniques to quantitatively estimate their impact on PIC's performance [17]. In the absence of such models, photonic

DfT techniques are desirable for testing and yield improvement via tuning/calibration. Similarly, on-chip phase monitoring [18] or post-fabrication trimming [19] is used for testing and calibration of PICs. On the other hand, test stations for semi-automatic wafer-level characterization of silicon photonic devices (fiber alignment, insertion loss, etc.) have been proposed in [7]. Similar developments for die and wafer level testing and probe access have been presented in [8] [9], using varied fiber coupling techniques.

While physical infrastructure development for testing and calibration of PICs has progressed, the advancement of CAD techniques and tools for photonic DfT and ATPG has been notably deficient. In this regard, in our previous work [10] [11], we have proposed photonic DfT architectures and circuits that enhance controllability and observability in devices under test for easier probing and measurements. The DfT architecture of [10] proposes MZI-based programmable couplers for capture of the test-response optical signal, which can be compared for power and phase against a reference laser. In contrast, [11] proposes ring-resonator (RR) based DfT architectures to: 1) inject test signals at the input of specific devices in the PIC, and 2) capture test responses at device outputs. The RR based architecture further allows *on-line testing by wavelength division multiplexing* of test signals of different wavelength than the normal operating wavelengths.

The above MZI or RR based DfT blocks have to be inserted at specific targets (devices or waveguides) in the PIC that are potentially more vulnerable to manufacturing variability and defects. However, to the best of our knowledge, there are no automated techniques and CAD tools available that can perform such a vulnerability localization in PICs – neither quantitatively nor qualitatively – for targeted DfT insertion. This paper addresses this gap in photonic test and DfT automation for test-point selection.

## III. Photonic Devices and Mismatch Parameters

Modern silicon photonic integrated circuits (PICs) leverage the high refractive-index contrast between silicon and its cladding (typically $SiO_2$) to densely integrate passive and active optical components [1]. This enables large-scale systems for data communication, computing, and sensing. Key building blocks include:

- **Waveguides:** Submicrometer silicon-on-insulator (SOI) waveguides form the interconnect backbone. Minimizing propagation loss requires careful management of factors like sidewall roughness, particularly in high-confinement structures [20], [21].
- **Couplers and MMIs:** Directional couplers utilize evanescent fields for power transfer, while multi-mode interferometers (MMIs) use interference for splitting/-combining signals.
- **Mach–Zehnder Interferometers (MZIs):** MZIs, composed of couplers and phase-shifting arms, perform modulation or switching [3]. Phase tuning often relies on the plasma dispersion effect via carrier injection/depletion in doped sections [22], altering the local refractive index.
- **Ring Resonators:** Compact looped waveguides create frequency-selective filters, modulators, or switches [2]. Their resonant condition is highly sensitive to variations in effective index, geometry, or temperature [21].
- **Photodetectors:** These devices convert optical signals back into electrical signals for processing. In silicon photonics, germanium-on-silicon (Ge-on-Si) photodiodes are widely used due to germanium's strong absorption at common telecommunication wavelengths (e.g., 1.31 µm, 1.55 µm) where silicon is transparent [23].

In the sequel, we use the following notation: $n_{\text{eff}}$ denotes the effective refractive index of a device, $\phi$ the phase, $\lambda$ the wavelength, and $\beta = \frac{2\pi n_{\text{eff}}}{\lambda}$ the propagation constant of the optical wave.

### A. Key Mismatch Parameters for DfT

The high sensitivity and dense integration that enable functionality also amplify the effects of manufacturing variations and operational drifts [4]. To develop a systematic DfT methodology, we identify and quantify key mismatch parameters, summarized in Table I. These parameters capture deviations from nominal design values.

TABLE I
Notation and Definitions of Key Mismatch Variables for DfT

| Symbol | Definition / Typical Ranges |
|---|---|
| $\Delta G_v$ | **Geometry deviation** [nm]: Waveguide width/thickness offsets (±2–10 nm). Affects $n_{\text{eff}}$, loss, coupling [4]. |
| $\Delta D_v$ | **Doping mismatch** [%]: Variation in dopant concentration (±3–5%). Affects carrier density, absorption, index shift [22], [24]. |
| $\Delta R_v$ | **Sidewall roughness** [nm]: Surface non-uniformity (≈ 5–10 nm). Major source of scattering loss [20]. |
| $\Delta T_v$ | **Temperature offset** [K]: Deviation from operating temperature (±5–10 K). Significant due to high thermo-optic coefficient of Si [5]. |
| $\Delta I_v$ | **Carrier injection drift** [mA]: Variation in drive current for modulators (±10%–30%). Affects modulation efficiency [24]. |
| $\Delta \alpha_v$ | **Thermal expansion/stress factor** [dimensionless]: Relevant for heater-based devices (typically ±5% of nominal) [4]. |
| $\Delta E_v$ | **Etch depth mismatch** [nm]: Variation in waveguide height (±5–10 nm). Affects mode profile and loss [21]. |
| $\Delta n_v$ | **Refractive index shift**: Material index changes (±0.001–0.005) due to doping, stress, etc. [22]. |
| $\Delta \phi_v$ | **Phase mismatch** [rad]: Error in coupler phase relationships (±0.1–0.5 rad). Affects interference devices. |
| $\Delta \lambda_v$ | **Wavelength offset** [nm]: Deviation from target wavelength (±1–3 nm). Critical for resonant devices [2]. |
| $\Delta P_v$ | **Polarization mismatch** [dB]: TE/TM imbalance (±1–2 dB). Relevant for polarization-sensitive designs. |
| $\Delta \text{MMI}_v$ | **MMI geometry mismatch** [nm]: Deviation from target MMI dimensions (±5–15 nm). |
| $L_e, B_e, T_e$ | **Waveguide Path Attributes:** Length, bend penalty, transition mismatch; respectively. Contribute to propagation loss and mode conversion [4]. |

### B. Sensitivity Coefficients ($\kappa$) and Data Sources

Each mismatch parameter $\Delta(\cdot)$ is linked to device performance through *sensitivity coefficients* $\kappa_{(\cdot)}$, quantifying the impact of a small perturbation. These crucial coefficients are obtained via:

1) **Foundry Process Data:** Process design kits (PDKs) often provide statistical variations, corner models, and empirical data linking parameters like $\Delta G_v$ or $\Delta R_v$ to performance metrics [25].
2) **Device Simulation (e.g., TMM):** Methods like the Transfer Matrix Method (TMM) allow calculating the partial derivatives of performance metrics with respect to mismatch parameters, yielding device-specific $\kappa$ values [12]. This is detailed further in Section V.

Understanding these sensitivities and their physical origins is fundamental to our risk assessment.

### C. Implications for Design-for-Test

This parameter-driven view directly informs DfT strategy:

- **Risk Identification:** Quantifying sensitivities ($\kappa$) highlights which parameters pose the greatest risk. This could be exploited for reliability, manufacturing aware redesign, or redesign with higher margins of sub-circuits.
- **Test Prioritization:** Components highly sensitive to dominant variations (e.g., a ring resonator sensitive to $\Delta T_v$ or $\Delta G_v$) become primary candidates for monitoring and test point insertion.
- **Calibration Needs:** Devices sensitive to operational drifts ($\Delta I_v, \Delta T_v$) may require built-in tuning mechanisms, and the sensitivity analysis helps identify where calibration points are most needed.

By grounding the DfT approach in these physical parameters and sensitivities, we move towards a more targeted and effective testing methodology.

## IV. Risk Weighting Heuristic

We model the PIC as a hypergraph $\mathcal{H} = (V, E)$, where photonic devices are nodes $v \in V$ and waveguide interconnects are hyperedges $e \in E$. Our DfT methodology relies on assigning quantitative risk weights to nodes and hyperedges within the PIC hypergraph. These weights reflect the component's sensitivity to physical mismatches and operational drifts (detailed in Section III), combined with its topological importance. This allows partitioning algorithms (Section VI) to identify high-risk sub-networks requiring targeted testing. Sensitivity coefficients ($\kappa$) derived from methods like TMM (Section V) or foundry data link physical parameters to performance impact.

### A. Node Weights ($W_{\text{device}}$)

The overall weight for a device node $v \in V$ comprises four main components:

$$W_{\text{device}}(v) = w_{\text{dev}}^{(v)} + w_{\text{tune}}^{(v)} + w_{\text{cent}}^{(v)} + w_{\text{coupling}}^{(v)}. \quad (1)$$

*1) Manufacturing Complexity $w_{\text{dev}}^{(v)}$:* Devices experience various fabrication mismatches, such as geometry deviation ($\Delta G_v$), doping error ($\Delta D_v$), sidewall roughness ($\Delta R_v$), etch depth mismatches ($\Delta E_v$), or refractive index shifts. We capture these sensitivity as manufacturing complexity.

$$w_{\text{dev}}^{(v)} = \kappa_{\text{geo}} \Delta G_v + \kappa_{\text{dose}} \Delta D_v + \kappa_{\text{rough}} \Delta R_v + \kappa_{\text{etch}} \Delta E_v + \kappa_{\text{index}} \Delta n_v + \dots \quad (2)$$

*2) Tuning Overhead $w_{\text{tune}}^{(v)}$:* Most integrated photonic devices rely on either *thermal tuning* or *carrier injection*. For thermal tuning, changes in temperature ($\Delta T_v$) or thermal expansion ($\Delta \alpha_v$) dominate. For doping or carrier-based modulators, injection drift ($\Delta I_v$) is crucial, and an additional *wavelength offset* ($\Delta \lambda_v$) might matter if the device is resonance-dependent. Thus we define two sub-weights:

$$w_{\text{inj}}^{(v)} = \kappa_{\text{inj}} |\Delta I_v| + \kappa_{\text{temp\_inj}} |\Delta T_v| + \kappa_{\lambda} |\Delta \lambda_v|, \quad (3)$$

$$w_{\text{th}}^{(v)} = \kappa_{\text{heat}} |\Delta T_v| + \kappa_{\text{exp}} |\Delta \alpha_v|. \quad (4)$$

Typically, a single device is often dominated by either injection or thermal tuning: $w_{\text{tune}}^{(v)} = \max(w_{\text{inj}}^{(v)}, w_{\text{th}}^{(v)})$ [5]. In designs combining multiple tuning mechanisms (e.g., doping plus heater trimming), designers may sum or weight both terms, depending on the device's actual strategy.

*3) Betweenness Centrality $w_{\text{cent}}^{(v)}$:* Topology of the interconnection network also contributes to test point selection. Certain devices, such as ring resonators or key Mach–Zehnder stages, can be "choke points" in the optical path. We quantify topological importance using betweenness centrality (BC) [26].

$$w_{\text{cent}}^{(v)} = \gamma_{\text{cent}} \cdot \text{BC}(v), \quad \text{BC}(v) = \sum_{s \neq v \neq t} \frac{\sigma_{st}(v)}{\sigma_{st}}. \quad (5)$$

Here, $\sigma_{st}$ is the number of shortest paths from node $s$ to node $t$, and $\sigma_{st}(v)$ is the fraction that passes through $v$. A higher value of $\text{BC}(v)$ implies that performance drifts in $v$ affect more optical paths, meriting a greater test focus. The user-defined scalar $\gamma_{\text{cent}}$ allows for tuning the relative contribution of the raw centrality score to the overall node weight calculation before normalization and aggregation with other risk factors (as described in Sec. IV-C).

*4) Coupler Mismatch $w_{\text{coupling}}^{(v)}$:* Devices often include directional couplers or MMIs. Let $\Delta \phi_v$ capture the phase mismatch in a directional coupler, $\Delta \text{MMI}_v$ the geometry offset in an MMI, and $\Delta P_v$ the polarization mismatch if the coupler is polarization-sensitive. Thus,

$$w_{\text{coupling}}^{(v)} = \kappa_{\text{dir}} |\Delta \phi_v| + \kappa_{\text{mmi}} \Delta \text{MMI}_v + \kappa_{\text{pol}} \Delta P_v. \quad (6)$$

If, for example, the device is polarization-insensitive, the $\kappa_{\text{pol}} \Delta P_v$ term can be dropped.

### B. Hyperedge Weights ($W_{\text{hyperedge}}$)

Waveguide segments comprising a hyperedge $e \in E$ are also weighted based on:

$$W_{\text{hyperedge}}(e) = w_{\text{loss}}^{(e)} + w_{\text{bend}}^{(e)} + w_{\text{transition}}^{(e)}. \quad (7)$$

- **Propagation Loss ($w_{\text{loss}}^{(e)}$):** $w_{\text{loss}}^{(e)} = \kappa_{\text{len}} \cdot L_e$ [20].
- **Bend Penalty ($w_{\text{bend}}^{(e)}$):** $w_{\text{bend}}^{(e)} = \kappa_{\text{bend}} \cdot B_e$.
- **Transition Mismatch:** $w_{\text{transition}}^{(e)} = \kappa_{\text{trans}} \cdot T_e$ [21].

### C. Aggregation, Normalization, and Scalar Tuning

Raw sub-weights are typically normalized (indicated by $\tilde{w}$) then combined using user-defined scalars $(\alpha, \beta, \gamma, \dots)$ based on foundry guidance [4], design goals, or TMM sensitivities ($\kappa$) to form the final weights $W_{\text{device}}$ and $W_{\text{hyperedge}}$:

$$W_{\text{device}}(v) = \alpha\, \tilde{w}^{(v)}_{\text{dev}} + \beta\, \tilde{w}^{(v)}_{\text{tune}} + \gamma\, \tilde{w}^{(v)}_{\text{cent}} + \zeta\, \tilde{w}^{(v)}_{\text{coupling}}, \tag{8}$$

$$W_{\text{hyperedge}}(e) = \alpha'\, \tilde{w}^{(e)}_{\text{loss}} + \beta'\, \tilde{w}^{(e)}_{\text{bend}} + \gamma'\, \tilde{w}^{(e)}_{\text{transition}}. \tag{9}$$

*Guidelines for Choosing Scalars $(\alpha, \beta, \gamma, \dots)$:* In practice, the scalars $(\alpha, \beta, \gamma, \zeta, \dots)$ can be chosen based on 1) *foundry guidance,* 2) *design goals* or 3) *partial derivatives from TMM*. For example, large partial derivatives $\partial r/\partial(\Delta G_v)$ imply geometry mismatch is critical, suggesting a higher weight for $\tilde{w}^{(v)}_{\text{dev}}$'s geometric terms. These total weights form the input for the partitioning stage (Section VI).

## V. Sensitivities via Transfer Matrix Method

The Transfer Matrix Method (TMM) is a numerical technique widely used in photonics to analyze how electromagnetic waves propagate through layered or cascaded optical components [27]. Each photonic element (waveguides, couplers, resonators) can be described by a matrix capturing its transmission and reflection. By multiplying these matrices sequentially, we form a composite matrix for the entire device. This allows efficient assessment of how small variations in manufacturing or operating conditions impact optical performance, crucially enabling the calculation of the sensitivity coefficients ($\kappa$) needed for our risk weighting heuristic (Section IV).

### A. Notation and Mismatch Parameters

Let $\Delta \equiv (\Delta G_v, \Delta D_v, \Delta I_v, \Delta T_v, \dots)$ be the vector of mismatch parameters (Table I). A device composed of $m$ sections has a composite $2 \times 2$ transfer matrix $T_{\text{device}}(\lambda, \Delta)$:

$$T_{\text{device}}(\lambda, \Delta) = \prod_{k=1}^{m} T_k(\lambda, \Delta). \tag{10}$$

Here, each individual matrix $T_k(\lambda, \Delta)$ depends on the operating wavelength $\lambda$ and the mismatch vector $\Delta$ because the physical properties (like effective index $n_{\text{eff},k}$ and absorption $\alpha_k$ in Eq. 11, or coupling coefficients) within section $k$ are functions of these mismatch parameters.

### B. Element 1: Straight Waveguide Section

A waveguide section matrix $T^{(\text{wg})}_k$ (Eq. 11) models propagation, modifying amplitude via loss $\alpha_k(\lambda, \Delta)$ and phase via propagation constant $\beta_k(\lambda, \Delta) = \frac{2\pi}{\lambda} n_{\text{eff},k}(\Delta)$ over length $L_k$. Both $\alpha_k$ and $\beta_k$ (through $n_{\text{eff},k}$) depend on $\Delta$ (e.g., $\Delta G_v, \Delta D_v, \Delta R_v, \Delta T_v$).

$$T^{(\text{wg})}_k(\lambda, \Delta) = \begin{pmatrix} e^{(-\frac{1}{2}\alpha_k + j\beta_k)L_k} & 0 \\ 0 & e^{(+\frac{1}{2}\alpha_k - j\beta_k)L_k} \end{pmatrix}. \tag{11}$$

### C. Element 2: Doped Phase Shifter / Injection Region

Phase shifters are modeled similarly, but $\alpha_k$ and $\beta_k$ explicitly incorporate sensitivities $\kappa^{(\cdot)}$ to relevant mismatches like doping $\Delta D_v$, injection current $\Delta I_v$, or geometry $\Delta G_v$, often linearized around a nominal point $\lambda_0$ (Eqs. 12, 13).

$$\alpha_k(\lambda, \Delta) \approx \alpha_0(\lambda) + \kappa^{(\text{dose})}_\alpha \Delta D_v + \kappa^{(\text{inj})}_\alpha \Delta I_v, \tag{12}$$

$$\beta_k(\lambda, \Delta) \approx \beta_0(\lambda) + \kappa^{(\text{dose})}_\beta \Delta D_v + \kappa^{(\text{inj})}_\beta \Delta I_v + \kappa^{(\text{geo})}_\beta \Delta G_v. \tag{13}$$

### D. Element 3: Directional Coupler or MMI

Coupling elements like directional couplers or 2x2 MMIs use a distinct transfer matrix $T^{(\text{dc})}_k$ (Eq. 14) whose complex elements $A_k, B_k, C_k, D_k$ capture the device's transfer function. These elements depend on device physics (e.g., coupling coefficient $\kappa_c$, length $L_k$) which are themselves functions of $\Delta$ (e.g., $\Delta G_v, \Delta\phi_v, \Delta\text{MMI}_v$).

$$T^{(\text{dc})}_k(\lambda, \Delta) = \begin{pmatrix} A_k(\lambda, \Delta) & B_k(\lambda, \Delta) \\ C_k(\lambda, \Delta) & D_k(\lambda, \Delta) \end{pmatrix}. \tag{14}$$

### E. Element 4: Ring Resonators and Reflectors

Resonant structures (e.g., ring resonators) are analyzed by cascading matrices of their constituent parts (couplers $T_c$, loop propagation $T_{loop}$) [2]. Their high sensitivity arises because mismatches $\Delta$ strongly affect loop phase (via $\beta_k(\Delta)$) and coupling (via $\kappa_c(\Delta)$), impacting resonant wavelength $\lambda_{\text{res}}(\Delta)$ and quality factor. Reflectors $r(\lambda, \Delta)$ are handled similarly. The TMM framework propagates $\Delta$-dependence throughout.

### F. Composite Device Matrix: Full Multiplication

The overall device transfer matrix $T_{\text{device}}(\lambda, \Delta)$ is the product of the individual section matrices (Eq. 10):

$$\begin{aligned} T_{\text{device}}(\lambda, \Delta) &= T_m(\lambda, \Delta) \times \cdots \times T_1(\lambda, \Delta) \\ &= \begin{pmatrix} A_{\text{dev}}(\Delta) & B_{\text{dev}}(\Delta) \\ C_{\text{dev}}(\Delta) & D_{\text{dev}}(\Delta) \end{pmatrix}. \end{aligned} \tag{15}$$

### G. Key Device Metrics from TMM

From the composite matrix $T_{\text{device}}(\lambda, \Delta)$, we calculate key performance metrics as functions of the mismatch vector $\Delta$.

*1) Insertion Loss and Phase:* Assuming minimal reflection ($S_{11} \approx 0$), the transmission S-parameter $S_{21} \approx 1/A_{\text{dev}}(\lambda, \Delta)$. The insertion loss (IL) as a function of mismatch is then:

$$\text{IL}(\Delta) = -10 \log_{10} |S_{21}(\Delta)|^2 \approx 20 \log_{10} |A_{\text{dev}}(\lambda, \Delta)| \quad \text{(dB)}. \tag{16}$$

Similarly, the net phase shift $\Phi(\Delta) = \arg(A_{\text{dev}}(\lambda, \Delta))$. Both $\text{IL}(\Delta)$ and $\Phi(\Delta)$ are now defined via the TMM result $A_{\text{dev}}(\Delta)$.

*2) Resonance Conditions:* For resonant structures like rings, resonance occurs when the round-trip phase is an integral multiple of $2\pi$, i.e. $2\pi n_{\text{eff}} L/\lambda = 2\pi m$, where $L$ is the circumference of the ring waveguide, and $m$ an integer. This corresponds to conditions like $\det[T_{\text{device}}(\lambda, \Delta)] = 1$ (for lossless) or derived from the eigenvalues or specific elements like $\arg(A_{\text{dev}}) = m \cdot 2\pi$ [2]. Solving this yields the resonant wavelength $\lambda_{\text{res}}(\Delta)$, which depends on mismatch parameters.

### H. Partial Derivatives and Sensitivity Coefficients ($\kappa$)

The sensitivity coefficients $\kappa$ for weighting (Sec. IV) are the partial derivatives of key performance metrics (e.g., IL, $\lambda_{\text{res}}$) with respect to individual mismatch parameters $\Delta_i \in \Delta$, evaluated at the nominal operating point ($\Delta = 0$):

*1) Insertion Loss Sensitivity:* Using Eq. 16,

$$\kappa_{\text{dose}}^{(\text{IL})} = \left.\frac{\partial(\text{IL})}{\partial(\Delta D_v)}\right|_{\Delta=0}, \quad \kappa_{\text{geo}}^{(\text{IL})} = \left.\frac{\partial(\text{IL})}{\partial(\Delta G_v)}\right|_{\Delta=0}, \dots \quad (17)$$

Units are typically dB/% (for $\Delta D_v$) or dB/nm (for $\Delta G_v$).

*2) Resonance Sensitivity:* For resonant devices:

$$\kappa_{\text{dose}}^{(\lambda)} = \left.\frac{\partial\lambda_{\text{res}}}{\partial(\Delta D_v)}\right|_{\Delta=0}, \quad \kappa_{\text{geo}}^{(\lambda)} = \left.\frac{\partial\lambda_{\text{res}}}{\partial(\Delta G_v)}\right|_{\Delta=0}, \dots \quad (18)$$

Units are typically nm/% or nm/nm. These quantify resonance shifts due to variations.

### I. Obtaining Sensitivity Coefficients ($\kappa$)

The sensitivity coefficients $\kappa = \partial(\text{Metric})/\partial(\Delta_i)|_{\Delta=0}$ (Sec. V-H) can be obtained via several methods: 1) **Numerical Differentiation:** Approximating derivatives from TMM metric outputs using finite differences. 2) **Symbolic Differentiation:** Computing exact derivatives from analytical TMM models using symbolic tools (e.g., SymPy). 3) **Foundry Data / PDK Models:** Extracting or inferring sensitivities from statistical models or corner simulations provided in PDKs [25]. Regardless of the method, the resulting $\kappa$ values quantify the physical link between process/operational variations ($\Delta$) and performance changes, directly informing the weighting heuristics (Sec. IV) [12].

## VI. Partitioning for Test Point Selection

Once the PIC is represented as a weighted hypergraph $\mathcal{H} = (V, E)$ with risk weights assigned to nodes and hyperedges (Section IV), the next critical step is partitioning this hypergraph. Partitioning segments the circuit into manageable sub-networks, allowing for the strategic placement of test resources (e.g., photodiodes, doping monitors, thermal sensors) [10]. The goal is to isolate sub-networks with the highest aggregated risk, concentrating testing efforts on components most susceptible to fabrication variations or operational drifts, thereby improving reliability and yield without excessive test overhead [6].

### A. Partitioning Goals: Coverage vs. Overhead

The effectiveness of a partition is evaluated based on two primary metrics:

- **Risk Coverage:** For a chosen sub-network (partition) $\mathcal{S} \subseteq (V \cup E)$, we define risk coverage as the fraction of the total PIC risk $W(\mathcal{H})$ captured within that partition:

$$\text{Risk Coverage}(\mathcal{S}) = \frac{W(\mathcal{S})}{W(\mathcal{H})}, \text{where} \quad (19)$$
$$W(\mathcal{S}) = \sum_{v\in\mathcal{S}} W_{\text{device}}(v) + \sum_{e\in E(\mathcal{S})} W_{\text{hyperedge}}(e).$$
$$W(\mathcal{H}) = \sum_{v\in\mathcal{H}} W_{\text{device}}(v) + \sum_{e\in E(\mathcal{H})} W_{\text{hyperedge}}(e).$$

  High coverage indicates that the partition contains a significant portion of the components deemed sensitive or critical.
- **Overhead $\mathcal{C}(\mathcal{S})$:** Instrumenting a partition $\mathcal{S}$ for DfT insertion incurs overhead in terms of area, insertion loss, power consumption, and routing complexity [4].

With the above weighted hypergraph model, we can envision the DfT selection as an optimization problem maximizing the net benefit:

$$\max_{\mathcal{S}} \left[W(\mathcal{S}) - \alpha_c \mathcal{C}(\mathcal{S})\right], \quad (20)$$

where $\alpha_c \in \mathbb{R}$ and $\alpha_c \geq 0$ balances the coverage-overhead trade-off. Achieving this involves several practical steps, starting with partitioning the hypergraph to effectively isolate high-risk regions.

### B. Partitioning Algorithms and KaHyPar

The core algorithmic step involves partitioning the risk-weighted hypergraph $\mathcal{H}$ into $k$ balanced blocks to group high-risk elements and minimize inter-partition connections. As this is an NP-hard problem to maximize Eqn. 20, finding the optimal solution is computationally intractable for large PICs. Therefore, we employ **KaHyPar** [13], a state-of-the-art multilevel partitioning tool that employs heuristics such as multilevel refinement and simulated annealing to efficiently find high-quality, near-optimal solutions.

In our experiments, KaHyPar is configured to optimize a cut metric based on inter-partition connectivity (specifically, the connectivity-1 or 'km1' metric in our implementation) subject to the node weight balance constraint defined by $k$ and $\epsilon$. This effectively isolates high-risk regions (addressing the $W(\mathcal{S})$ component of Eqn. (20)), as it tends to keep high-risk components together. The overhead component $\mathcal{C}(\mathcal{S})$ is managed separately via budget constraints during TIP selection (Sec. VI-C). Key parameters remain the number of partitions ($k$) and the balance factor ($\epsilon$), which ensures partitions $P_i$ satisfy $W(P_i) \leq (1+\epsilon)W(\mathcal{H})/k$, where $0 < \epsilon < 1$.

### C. Test Point Selection Methodology

Following hypergraph partitioning, this methodology provides a systematic approach to select Test Insertion Points (TIPs) based on quantitative metrics derived from the weighted hypergraph and the partitioning solution, while respecting resource constraints.

*1) Node Prioritization Based on Risk and Topology:* Once partitions are defined based on the overall risk weights (which include a centrality component as described in Sec. IV), we compute a separate 'NodeScore' to prioritize individual nodes for TIP placement. This score explicitly re-evaluates the node's overall calculated risk ($\tilde{W}_{\text{device}}(v)$) alongside its normalized topological centrality ($\tilde{\text{BC}}(v)$) [26] to guide the selection process:

$$\text{NodeScore}(v) = \alpha_N \cdot \tilde{W}_{\text{device}}(v) + \beta_N \cdot \tilde{\text{BC}}(v) \quad (21)$$

Here, $\tilde{W}_{\text{device}}(v)$ is the normalized total device risk weight from Eq. 8, and $\tilde{\text{BC}}(v)$ is the normalized betweenness centrality. The user-defined factors $\alpha_N$ and $\beta_N$ allow tuning the relative emphasis between overall device risk and pure topological importance specifically for the TIP selection stage. This scoring provides a unified metric to rank potential monitoring locations.

*2) Identifying and Ranking Candidate TIPs:* With node scores computed, candidate TIPs are identified from two primary sources: high-risk regions within partitions and critical boundaries between partitions.

- **Internal Candidates:** Partitions ($P_i$) whose aggregated risk ($W(P_i)$) exceeds a predefined threshold ($R_{thresh} = \theta \cdot W(\mathcal{H})$) are identified as "high-risk". Within each such partition, the node possessing the highest 'NodeScore' is selected as a primary candidate for internal monitoring. These candidates across all high-risk partitions form a ranked list ($L_{internal}$).
- **Boundary Candidates:** Hyperedges crossing partition boundaries ($E_{cut}$) whose weights ($W_{\text{hyperedge}}(e)$) exceed a significance threshold ($W_{cut\_thresh}$) are deemed high-priority. For each such hyperedge $(u, v)$, the adjacent node ($u$ or $v$) that resides in the higher-risk partition (or has a higher 'NodeScore' if risks are similar) is considered a potential boundary TIP location ($v_{e,TIP}$). These locations are ranked ($L_{boundary}$), typically based on the weight of the associated cut hyperedge.

*3) Budget-Constrained TIP Selection:* The final set of TIPs ($S_{TIP}$) is determined by selecting from the ranked candidate lists ($L_{internal}$ first, then $L_{boundary}$) while adhering to the test overhead budget ($C_{budget}$). A candidate node is added to $S_{TIP}$ only if it is not already included and if its associated cost ($Cost(TIP)$) fits within the remaining budget. This ensures the highest-priority locations are selected preferentially.

It is important to note that selecting a node $v$ as a TIP implies placing a specific test structure (e.g., a monitor or injection point) associated with the device represented by $v$. This provides targeted observability or controllability at that critical location.

### D. Overhead Calculation and Iteration

After determining $S_{TIP}$ and selecting a TIP strategy, calculate the total estimated overhead $\mathcal{C}(S_{TIP})$.

- **Cost Calculation:** Sum the overhead contributions (area, insertion loss, power) from each TIP in $S_{TIP}$ and the chosen TIP implementation.
- **Budget Check:** Compare $\mathcal{C}(S_{TIP})$ against the initial budget $C_{budget}$.
- **Iteration:** If $\mathcal{C}(S_{TIP}) > C_{budget}$, the process must be iterated (e.g., by raising thresholds, adjusting score weights, reducing TIP count, revisiting partitioning parameters, or re-evaluating the TAP strategy).

This iterative refinement ensures the final DfT plan meets overhead constraints. Test structures (photodiodes, taps, sensors) introduce overhead (Area, Loss/Crosstalk, Power/Thermal budget). We encapsulate these into a cost function $\mathcal{C}(\mathcal{S})$ used in partitioning (Eq. 20).

## VII. Our Implementation Flow and Automation

Deploying the proposed physics-informed DfT methodology effectively requires integration with standard Electronic Design Automation (EDA) and Photonic Design Automation (PDA) workflows [28]. The methodology leverages PDK resources: Device Libraries/Models, Process Variation Data (including corner models [4], [29]), and Design Rules (DRCs). Integration uses custom scripts/plugins within common EDA/PDA tool environments to parse layouts, extract parameters, access PDK data, and manage the DfT flow [30]. Our implementation follows a structured sequence:

1) **Collect Coefficients:** Gather $\kappa$ values from TM-M/PDKs.
2) **Parse Layout:** Extract parameters hierarchically [28].
3) **Assemble Weighted Hypergraph:** Construct $W_{\text{device}}$ and $W_{\text{hyperedge}}$.
4) **Automated Partitioning:** Run KaHyPar [13] $(k, \epsilon)$.
5) **TIP Selection & Overhead Analysis:** Apply criteria from Sec. VI-C. Estimate $\mathcal{C}(\mathcal{S})$.
6) **Place Test Structures & Refine:** Insert DfT monitors/-taps. Iterate if overhead budget is exceeded.

## VIII. Experimental Setup and Results

To validate the effectiveness of the proposed risk-weighted DfT methodology, we have implemented the workflow using Python, associated libraries (e.g. NetworkX, Matplotlib), and KaHyPar [13]. We compared unweighted vs. weighted partitioning on three PIC benchmarks.

- **Weighting:** Based on Sec. IV, representative $\kappa$ values taken from [4], [24], and Table I ranges. Hyperedge weights derived from path attributes.
- **Partitioning:** KaHyPar, $k \in \{2, 3\}$, $\epsilon = 0.05$.
- **Overhead Model:** Cost overhead metrics are taken from the design characteristics of the DfT blocks designed in our previous work [10] [11].

We evaluated three distinct PIC designs, represented as hypergraphs for partitioning:

*1) Example 1: 4×4 Photonic Switch Fabric with Rings and MZIs:* Design inspired from [31], the weighted graph for this switch (Total Risk: 43.607) is shown in Figure 1. Parameters influencing the weights are detailed in Tables II and III. Figure 2 shows the $k = 2$ partitioning. The higher-risk stage, including rings, is isolated into one partition, achieving

TABLE II
NODE-LEVEL MISMATCH PARAMETERS USED IN EXAMPLE1

| **Node** | $\Delta G_v$ | $\Delta D_v$ | $\Delta R_v$ | $\Delta I_v$ | $\Delta T_{inj}$ | $\Delta \lambda_v$ | $\Delta \phi_v$ | $\Delta \text{MMI}_v$ |
|---|---|---|---|---|---|---|---|---|
| I1 | 2.8 | 0.0 | 4.1 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| I2 | 3.5 | 0.0 | 3.2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| I3 | 3.9 | 0.0 | 6.8 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| I4 | 1.9 | 0.0 | 2.4 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| MMI1 | 9.5 | 4.5 | 7.6 | 0.0 | 6.4 | 0.0 | 0.0 | 10.8 |
| MMI2 | 2.7 | 4.0 | 6.3 | 0.0 | 9.5 | 0.0 | 0.0 | 13.1 |
| MZ1 | 4.8 | 4.0 | 6.3 | 0.3 | 8.3 | 2.9 | 0.1 | 0.0 |
| MZ2 | 9.6 | 3.5 | 5.0 | 0.3 | 10.0 | 2.3 | 0.1 | 0.0 |
| MZ3 | 5.9 | 4.8 | 5.2 | 0.5 | 5.9 | 1.5 | 0.5 | 0.0 |
| MZ4 | 5.1 | 4.6 | 8.2 | 0.4 | 8.2 | 2.8 | 0.5 | 0.0 |
| O1 | 4.5 | 0.0 | 2.3 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| O2 | 2.5 | 0.0 | 3.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| O3 | 1.4 | 0.0 | 3.7 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| O4 | 4.8 | 0.0 | 4.0 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| R1 | 6.1 | 4.2 | 8.2 | 0.05 | 7.9 | 1.3 | 0.5 | 0.0 |
| R2 | 3.5 | 4.4 | 5.7 | 0.1 | 9.1 | 1.2 | 0.2 | 0.0 |

TABLE III
HYPEREDGE-LEVEL PATH ATTRIBUTES USED IN EXAMPLE1

| **Hyperedge** | $L_e$ **(mm)** | $B_e$ **(bends)** | $T_e$ **(trans)** |
|---|---|---|---|
| I1–MMI1 | 0.3 | 1 | 3.6 |
| I2–MMI1 | 0.7 | 3 | 1.6 |
| I3–MMI1 | 0.2 | 0 | 3.8 |
| I4–MMI1 | 0.4 | 2 | 0.6 |
| MMI1–MZ1 | 0.9 | 0 | 4.8 |
| MMI1–MZ2 | 0.3 | 0 | 2.0 |
| MMI2–MZ1 | 0.3 | 2 | 3.4 |
| MMI2–MZ2 | 0.8 | 0 | 1.7 |
| MMI2–MZ3 | 1.0 | 4 | 2.9 |
| MMI2–MZ4 | 1.0 | 4 | 3.2 |
| MZ3–R1 | 0.6 | 3 | 2.7 |
| MZ4–R2 | 0.9 | 4 | 4.3 |
| O1–R1 | 1.0 | 3 | 1.3 |
| O2–R1 | 1.0 | 0 | 4.6 |
| O3–R2 | 0.9 | 4 | 3.5 |
| O4–R2 | 0.8 | 2 | 1.3 |

45.7% Max Cov (Table IV). Cut edges (dashed orange) bridge the two stages. $S_{TIP}$ is {MMI1, MMI2, MZ3} (red borders), comprising 2 internal and 1 boundary candidate, corresponding to a cut cost (C. Cost) of 4.103. Figure 3 displays the $k = 3$ partitioning. Finer subdivision occurs, reducing Max Cov to 38.1% but increasing the cut cost to 6.342 (Table IV). The $S_{TIP}$ for $k = 3$ is {MMI1, MMI2, MZ4}, requiring 3 TIPs (3 internal, 0 boundary) to monitor the fragmented high-risk areas in this run.

*2) Example 2: Photonic Neural Network (PNN):* Design inspired from [32], this $6 \times 6$ MZI array (Total Risk: 215.075) is shown weighted in Figure 4. For $k = 2$ (Figure 5), the grid divides into two partitions with 49.3% Max Cov and a cut cost of 10.325 (Table IV). $S_{TIP}$ is {MZ(3,4), MZ(4,2), MZ(4,4)} (3 TIPs: 2 internal, 1 boundary). For $k = 3$ (Figure 6), the grid divides into three sections. Max Cov drops to 32.3%, while the cut cost increases to 17.885. $S_{TIP}$ becomes {MZ(2,4), MZ(3,4), MZ(3,5), MZ(4,2)} (4 TIPs: 3 internal, 1 boundary), targeting nodes across the refined partitions.

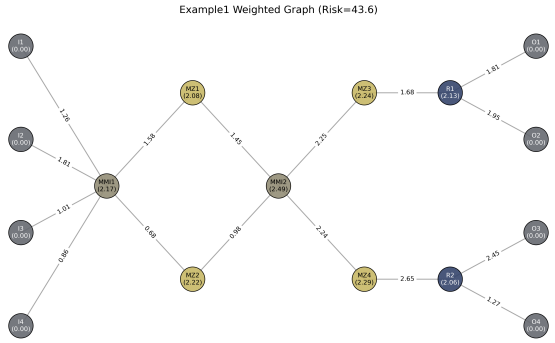


Fig. 1. Weighted $4 \times 4$ Photonic Switch with Rings (Example 1 - Visualization)

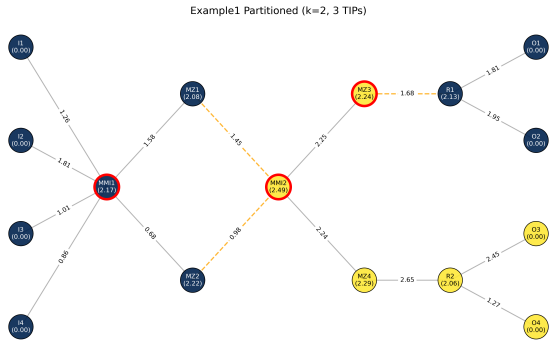


Fig. 2. Partitioning (k=2) of Weighted Switch Hypergraph (Example 1)

*3) Example 3: Medium-Complexity Hybrid Integration Benchmark:* This benchmark network (Total Risk: 67.265) includes mixed device types (Figure 7). The $k = 2$ partitioning (Figure 8) achieves 38.1% Max Cov with a cut cost of 16.208 (Table IV). $S_{TIP}$ is {MMI2, MZ1, MZ2} (3 TIPs: 2 internal, 1 boundary), targeting high-risk or boundary-adjacent nodes. With $k = 3$ (Figure 9), the network splits into three, reducing Max Cov to 24.0% and increasing the cut cost to 22.569. $S_{TIP}$

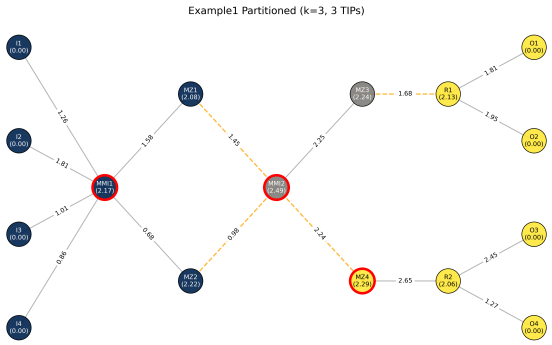


Fig. 3. Partitioning (k=3) of Weighted Switch Hypergraph (Example 1)

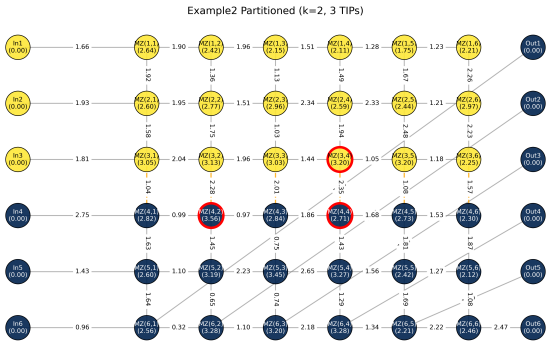


Fig. 5. Partitioning (k=2) of Weighted PNN Hypergraph (Example 2)

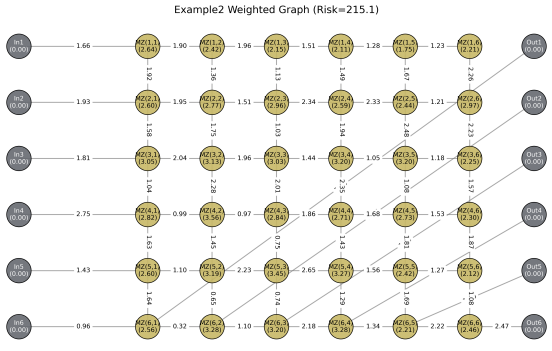


Fig. 4. Weighted Photonic Neural Network (Example 2 - Visualization)

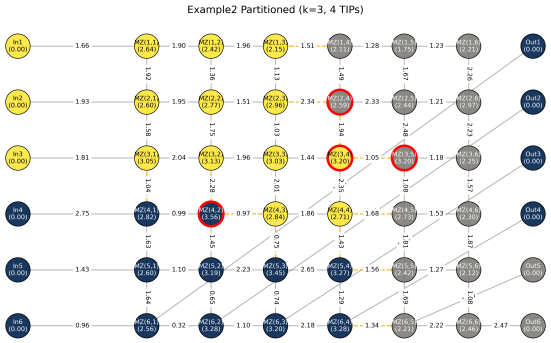


Fig. 6. Partitioning (k=3) of Weighted PNN Hypergraph (Example 2)

expands to {MMI1, MZ2, MZ4, MZ6} (4 TIPs: 3 internal, 1 boundary) to cover the distributed risk within budget.

### A. Consolidated Results and Discussion

The quantitative outcomes presented in Table IV and visualized in Figures 1–9 validate the proposed DfT methodology across different PIC designs modeled as hypergraphs. The table utilizes overhead cost assumptions from [10] and detailed in Table V.

**Effectiveness of Weighted Partitioning:** The primary benefit of the weighting heuristic is evident when comparing the targeted results to an unweighted baseline. By incorporating device and interconnect sensitivities derived from mismatch values (Tables II, III for Example 1) and sensitivity coefficients, the partitioning algorithm successfully identifies and isolates components contributing most significantly to the overall circuit risk (Total Risk values of 43.607, 215.075, and 67.265 for Examples 1, 2, and 3, respectively). For instance, in the $4 \times 4$ switch (Fig. 1), the high weights assigned to specific rings and MZIs lead KaHyPar to group these elements. As shown for k=2 (Fig. 2), one partition captures a substantial portion of this risk (Max Cov 45.7%). Similarly, the PNN (Fig. 4) and medium-complexity benchmark (Fig. 7) show effective isolation of higher-weighted components in the k=2 partitioning (Figs. 5, 8). This confirms that physics-informed weighting directs partitioning towards functionally critical or variation-sensitive components.

**Impact of k-Way Partitioning and TIP Selection:** The use of k-way partitioning allows for finer granularity in sub-circuit localization compared to simple bipartitioning (k=2). Comparing the k=2 and k=3 results in Table IV highlights this trade-off. Increasing k generally decreases the maximum risk coverage within any single partition (e.g., Ex1: 45.7% to 38.1%; Ex2: 49.3% to 32.3%; Ex3: 38.1% to 24.0%) because the risk is distributed among more, smaller partitions. This finer granularity, however, comes at the cost of increased partitioning complexity, reflected in the significantly higher Cut Cost (C. Cost) values for k=3 compared to k=2 across all examples (e.g., Ex1: 4.103 to 6.342; Ex2: 10.325 to 17.885; Ex3: 16.208 to 22.569). Correspondingly, the TIP selection strategy adapts: the number of selected TIPs ($|S_{TIP}|$) increases from 3 to 4 only for Examples 2 and 3 when moving from k=2 to k=3 (Example 1 remains at 3 TIPs for k=3 in this run), reflecting the need to monitor more partitions or boundaries to satisfy the selection criteria within the given budget. The TIPs (I/B) column shows the breakdown, indicating that the selection includes both internal high-risk nodes and boundary nodes The specific TIPs selected (listed in the final column and visualized in Figs. 2, 3, 5, 6, 8, 9) confirm placement within high-risk partitions or adjacent to significant cut edges.

**Overhead Considerations:** Table IV quantifies the estimated overhead (Area/Power/Loss) based on the number of selected TIPs ($|S_{TIP}|$) and the per-TIP costs assumed in

TABLE IV
CONSOLIDATED RESULTS FROM PYTHON IMPLEMENTATION

| Ex. | k | T. Risk | Cov (%) | Overhead (A/P/L) | $\lvert S_{TIP} \rvert$ | TIPs (I/B) | C. Cost | Time (s) | Selected TIPs ($S_{TIP}$) |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 43.607 | 45.7 | A:126669/P:150.0/L:7.8 | 3 | 2/1 | 4.103 | 0.001 | MMI1, MMI2, MZ3 |
| 1 | 3 | 43.607 | 38.1 | A:126669/P:150.0/L:7.8 | 3 | 3/0 | 6.342 | 0.001 | MMI1, MMI2, MZ4 |
| 2 | 2 | 215.075 | 49.3 | A:126669/P:150.0/L:7.8 | 3 | 2/1 | 10.325 | 0.006 | MZ(3,4), MZ(4,2), MZ(4,4) |
| 2 | 3 | 215.075 | 32.3 | A:168892/P:200.0/L:10.4 | 4 | 3/1 | 17.885 | 0.008 | MZ(2,4), MZ(3,4), MZ(3,5), MZ(4,2) |
| 3 | 2 | 67.265 | 38.1 | A:126669/P:150.0/L:7.8 | 3 | 2/1 | 16.208 | 0.002 | MMI2, MZ1, MZ2 |
| 3 | 3 | 67.265 | 24.0 | A:168892/P:200.0/L:10.4 | 4 | 3/1 | 22.569 | 0.003 | MMI1, MZ2, MZ4, MZ6 |

Note: Cov is highest risk coverage fraction among partitions. Overhead (A/P/L): Area $\mu m^2$/Power mW/Loss dB per TIP. $\lvert S_{TIP} \rvert$: Number of selected TIPs. TIPs (I/B): Internal/Boundary TIP count breakdown. C. Cost: Weighted cut cost (sum of weights of inter-partition edges). Time: KaHyPar partitioning duration in seconds. $S_{TIP}$ lists selected nodes.

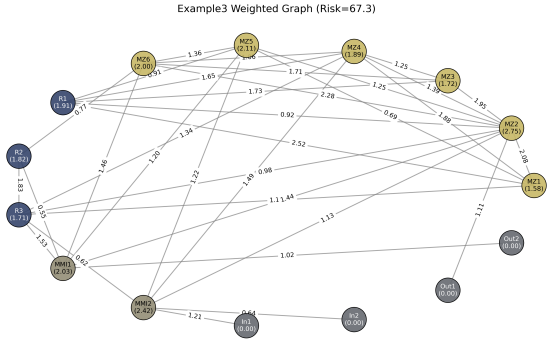


Fig. 7. Weighted Medium-Complexity Benchmark (Example 3 - Visualization)

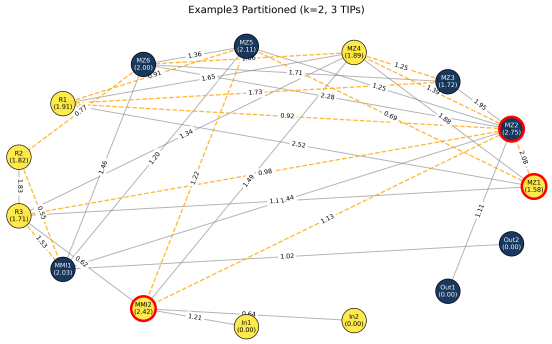


Fig. 8. Partitioning (k=2) of Weighted Benchmark Hypergraph (Example 3)

TABLE V
PHYSICAL OVERHEAD COSTS PER TEST INSERTION POINT [10], [11]

| Overhead Component | Value | Unit |
|---|---|---|
| Area | 42223 | $\mu m^2$ |
| Est. Power (static, $\pi$) | 50.0 | mW |
| Insertion Loss | 2.6 | dB |

Table V. The results demonstrate that substantial risk coverage (approx. 24% to 49% Max Cov) is achieved with a quantifiable overhead. As expected, where 'k' increases from 2 to 3 and results in more TIPs (Examples 2 and 3), there is a corresponding increase in overhead (e.g., Area increases from

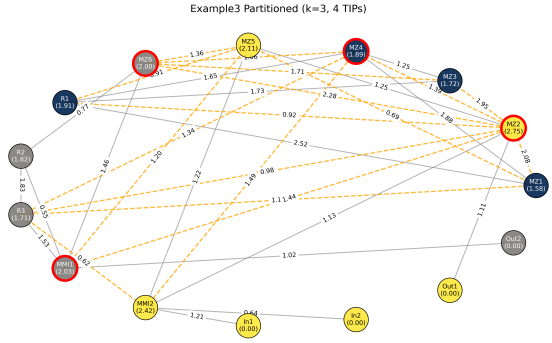


Fig. 9. Partitioning (k=3) of Weighted Benchmark Hypergraph (Example 3)

126669 $\mu m^2$ to 168892 $\mu m^2$).

**KaHyPar Performance:** The visual results (Figs. 2–9) confirm that KaHyPar generates balanced partitions (with $\epsilon = 0.05$) that visually group high-weight nodes. Table IV provides the Cut Cost (C. Cost) metric produced by the heuristic algorithm for each case, offering a quantitative measure of the partitioning quality achieved while respecting the balance constraint. The partitioning compute times are also listed, showing the efficiency of the approach (ranging from 0.001s to 0.008s in these examples).

In summary, the experimental results, detailed in Table IV, demonstrate that the combination of physics-informed risk weighting and balanced k-way partitioning provides a powerful and adaptable DfT strategy.

## IX. CONCLUSION

We have presented and demonstrated a comprehensive, weighted DfT framework tailored for silicon photonic integrated circuits. By explicitly unifying node-level (device) and hyperedge-level (waveguide interconnect) mismatch parameters, informed by physically derived sensitivity coefficients ($\kappa$) from TMM simulations or foundry process data, our methodology provides a quantitative basis for risk assessment. It translates variations in geometry, doping, roughness, and operational conditions into actionable risk weights, addressing the reality that PIC failures often stem from a combination of device-specific issues and interconnect vulnerabilities.

The core strength lies in coupling this physics-informed weighting with automated, balanced k-way hypergraph partitioning using tools like KaHyPar [13]. This enables the systematic identification and isolation of high-risk sub-networks within complex PIC layouts. As demonstrated through examples including MZI-based switches [31] and ring resonators [2], this approach significantly enhances controllability and observability, and allows for targeted test point insertion, achieving substantial risk coverage with moderate, quantifiable overhead. Future directions include enhancing the weighting model to explicitly incorporate polarization and WDM effects, and investigating calibration based on monitored results.

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