

# Testing & Verification of Digital Circuits

ECE/CS 5745/6745

## *Hardware Verification using Symbolic Computation*

- Instructor: Priyank Kalla (kalla@ece.utah.edu)
- 3 Credits
- Mon, Wed 1:25 - 2:45pm, JTB 110
- Office Hours: Tue: 12pm - 1pm, or by appointment
- HWs and Programming Assignments + 1 term-project
- Textbook: I'm writing a textbook, which will be provided to you for free! All lecture slides will be provided
- Reference books listed on the class website

## Course Websites

Two resources for course website:

- The course material will be available at:

[http://www.ece.utah.edu/~kalla/index\\_6745.html](http://www.ece.utah.edu/~kalla/index_6745.html)

- A Canvas link to course website is also provided:

## Agenda for Today

- Introduction to Test, Validation & Verification
- Course Syllabus Overview
- Course Organization
- Requirements, Responsibilities, grading policy, etc.
- Discussions....

## Course Organization

- Grading Policy: HW: 60%; Project - 40%
- Course Materials: Lecture notes, slides, tutorials, and papers
- [http://www.ece.utah.edu/~kalla/index\\_6745.html](http://www.ece.utah.edu/~kalla/index_6745.html)
- HW submissions through Canvas
- Pre-requisites: Basic Digital Design + programming experience  
- I'll teach the rest!
- HW: some problem solving + some experiments with tools + some CAD tool programming and design.
- Projects: Theoretical study, experiments, CAD tool implementation, preliminary investigations on a research problem...

## VLSI Circuit Realization Process

- Customer's requirements
- Design Conceptualization by customers and designers
- Design Specifications (usually in English)
- Design Descriptions - VHDL, Verilog, SystemC, ...
- Circuit realization: Synthesis, Custom Design
- Marketing.....
- Where do Test and Verification fit-in?

# VLSI Circuit Realization Process

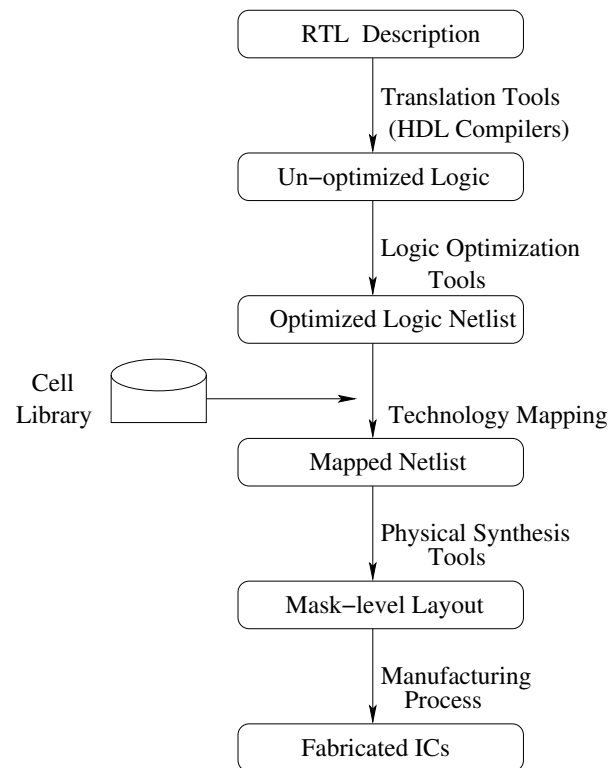


Figure 1: The VLSI Realization Process: A Typical design synthesis flow.

# Design Validation

- Is the **specification** fool-proof?
  - Bugs: mis-understanding, incorrect modeling, oversight...
  - How to ascertain validity of the specs?
  - Simulate (randomly?) and observe ... too slow
  - Mathematically infer validity..... computationally complex
  - Today's solutions: little-bit of math + little-bit of simulation + little-bit of luck!
- Topics on design validation: Simulation, coverage metrics, property verification, model checking, among others..

# Enhancing the Power of Simulation

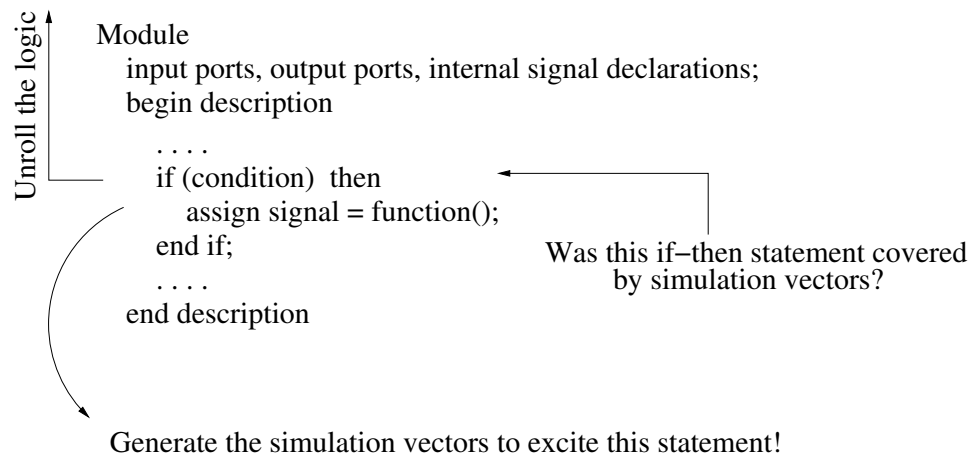


Figure 2: Enhancing RTL code coverage.



# Formal Design Verification

- Simulation is incomplete
  - Mathematicians say: “Mathematically prove that your system is fool-proof!”
  - Theorem Proving and Model Checking.....
  - Computationally complex, but great progress in the past decade
  - Proof of equivalence is (somewhat) manageable
  - Industry tools available for equivalence and model checking
  - Our focus: Implementation Verification via Equivalence Checking

# Verification: Equivalence Checking

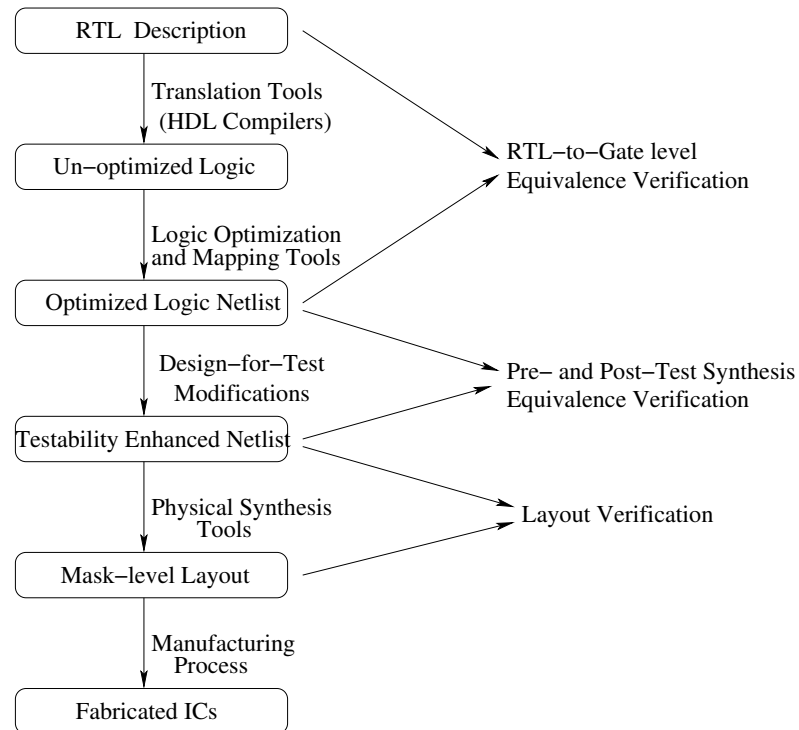


Figure 3: Typical implementation verification flow.

# Equivalence Checking Setup

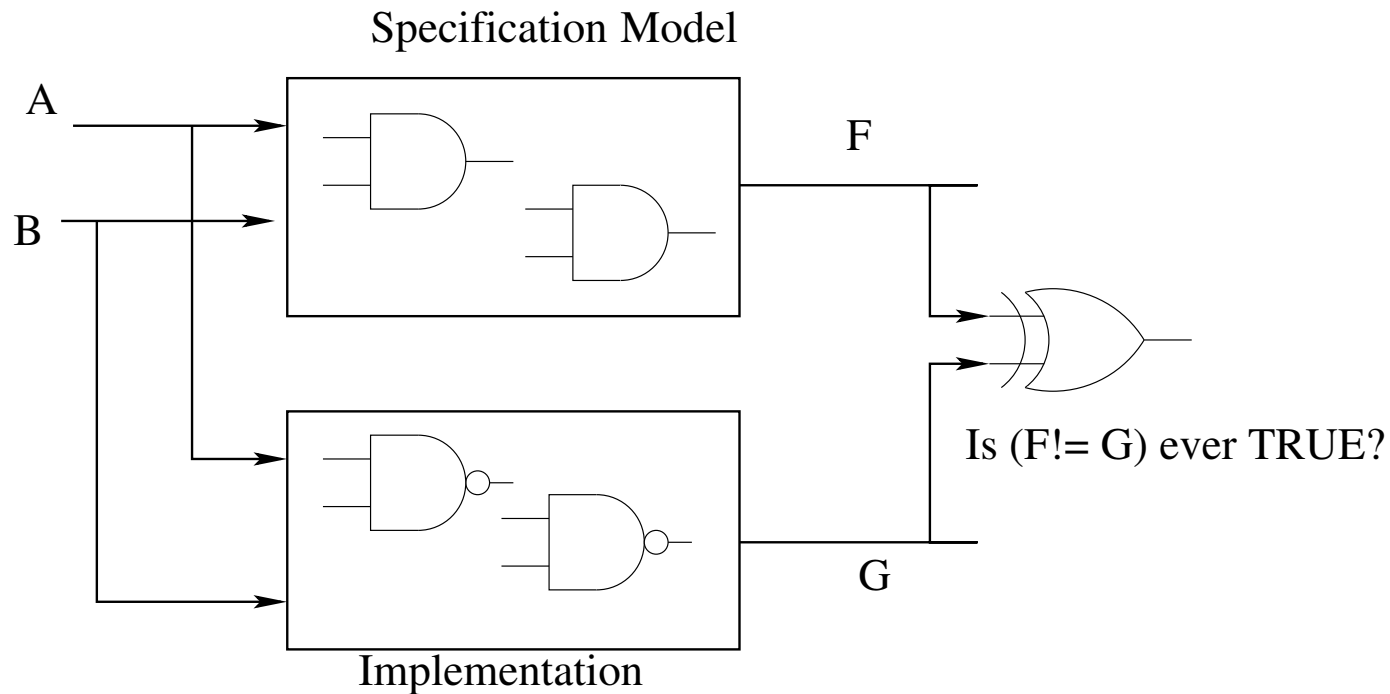


Figure 4: Equivalence Checking Setup: A Miter

## Equivalence Checking Examples

```
module verify(a, b, c, f, y, X, Z, F)
input a, b, c; // Boolean
input [3:0] X; // Bit-vectors
output f, y;
output [3:0] F, Z;

assign f = a'bc + ab'c + abc' + abc;
assign y = ab + ac + bc; // a(b+c) + bc

assign F[3:0] = 8 * X[3:0] * X[3:0] + 8* X[3:0];
assign Z[3:0] = 4'b0000;
```

## VLSI Testing

- Testing a fabricated chip for manufacturing defects.
- Physical Failures and Fabrication Defects due to:
  - Shorts or opens on wires.... unreliable metalization
  - Electromigration over a period of time
  - Shorts (fusing) of Source-Drain
  - Improper ion-implantation... slow switching
  - Ever heard of latch-up?
  - Reliability of a manufacturing process in general
- Will also study some VLSI testing fundamentals in the course