Testing and Verification of Digital Circuits
ECE/CS 5745/6745 – Fall 2025

Some make-up questions for HW 4 (Qs 1, 2, &3)
Due date: Fri Dec 5
Instructor: Priyank Kalla

These are make-up questions for Qs 1, 2, & 3 in HW4. So if you got any of those wrong, you may solve these instead, and I'll replace your grade with the better grade for each of these questions.

1) **[Multi-fault ATPG: 15 points]** Consider the circuit of Fig. 1.

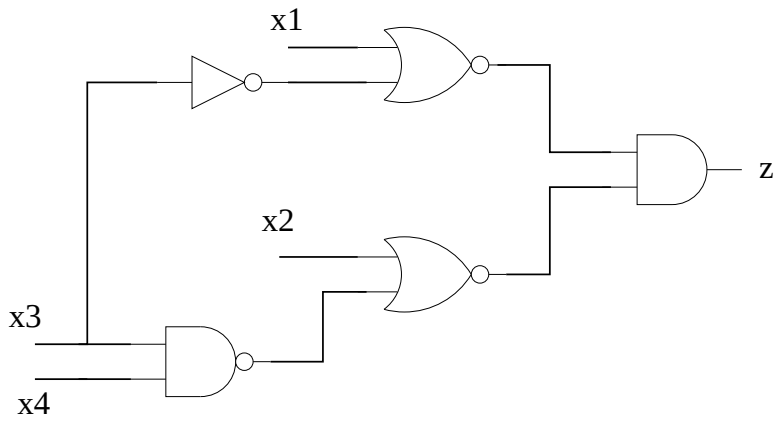

Fig. 1. The circuit to test for single- and multi-faults

a) Find a test for single fault x_3 stuck-at-1 ($x_3/1$).
b) Find a test for single fault x_2 stuck-at-0 ($x_2/0$).
c) Find a test for the multi-fault $\{x_3/1, x_2/0\}$.
d) Does the multi-fault scenario invalidate the single-stuck-fault testing assumptions? Explain.

2) **[Fault Collapsing: 25 points]** For the circuit shown in Fig. 2.

a) (10 pts) Suppose we wish to derive a set of tests to *distinguish* between all distinguishable single stuck-at faults in the circuit of Fig. 2. Identify a set of faults for which tests *need not* be derived.
b) (5 pts) List all the checkpoint faults of this circuit.
c) (10 pts) Find a *smallest/minimal* subset of checkpoint faults that must be targeted for test generation if the *detection* of all single stuck-at faults is the goal.

3) **[Stuck-at faults at fanout stems and branches: 20 points]** For the circuit shown in Fig. 2:

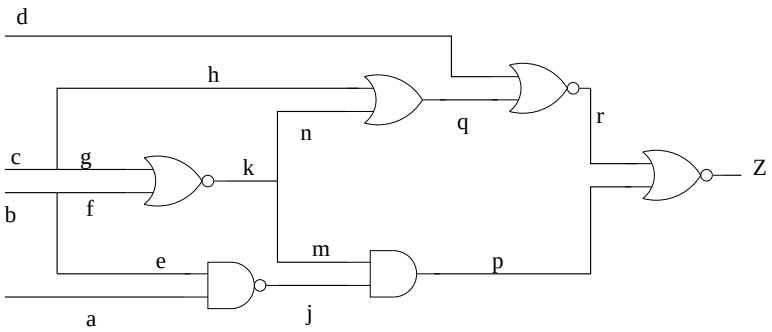

Fig. 2. The circuit diagram related to checkpoint faults, and to test k, m, n s-a-0

a) Derive a test for the stuck-at-faults: (i) $k/0$; (ii) $m/0$; (iii) $n/0$ using path sensitization. First attempt single path sensitization; and only then try multiple path sensitization, if needed.

b) If any of the above faults is/are undetectable, remove the redundancy and simplify the circuit. Do not use Boolean algebra!