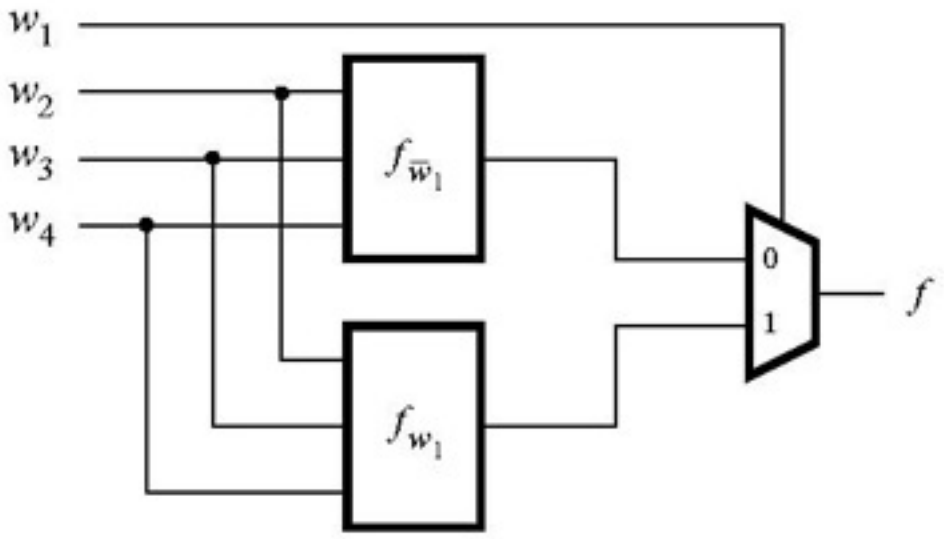
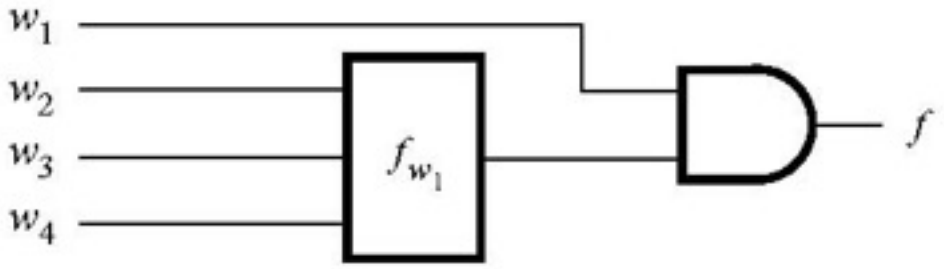
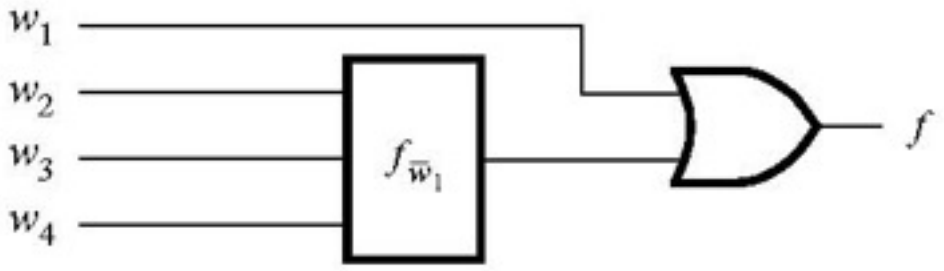


(a) Shannon's expansion of the function *f*.

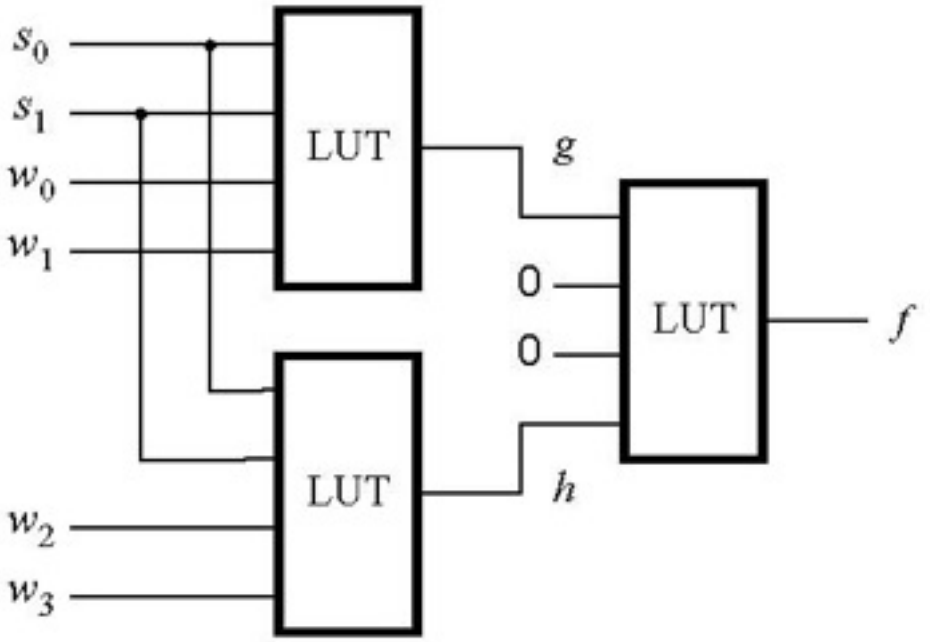


(b) Solution for part *a*

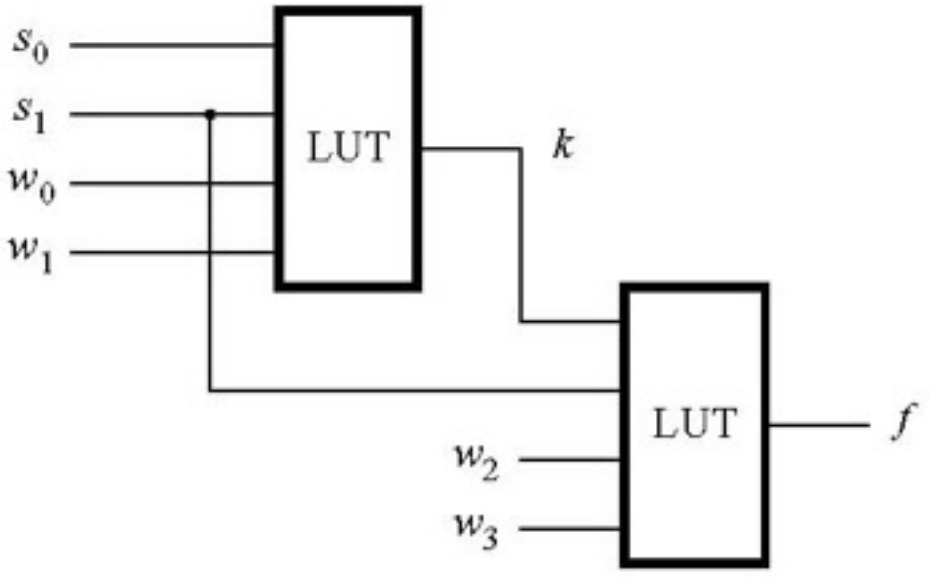


(c) Solution for part *b*

Figure 4.48. Circuits for Example 4.28.



(a) Using three LUTs



(b) Using two LUTs

Figure 4.49. Circuits for Example 4.29.

```
module mux4to1 (W, S, f);
    input [0:3] W;
    input [1:0] S;
    output f;
    wire [0:3] Y;

    dec2to4 decoder (S, 1, Y);
    assign f = |(W & Y);
endmodule


module dec2to4 (W, En, Y);
    input [1:0] W;
    input En;
    output reg [0:3] Y;

    always @(W, En)
        case ({En, W})
            3'b100: Y = 4'b1000;
            3'b101: Y = 4'b0100;
            3'b110: Y = 4'b0010;
            3'b111: Y = 4'b0001;
            default: Y = 4'b0000;
        endcase
endmodule
```

Figure 4.52. Verilog code for Example 4.32.