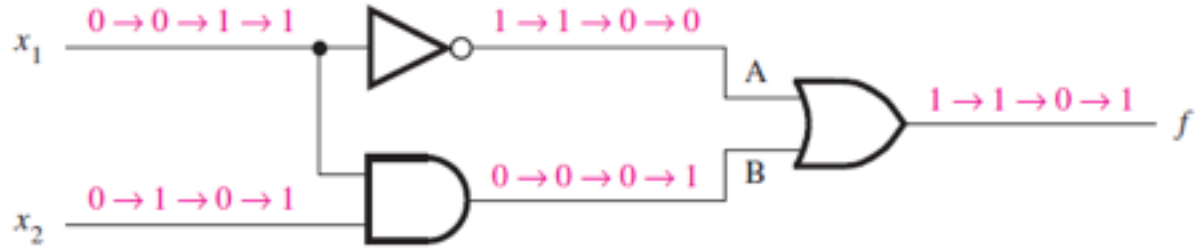
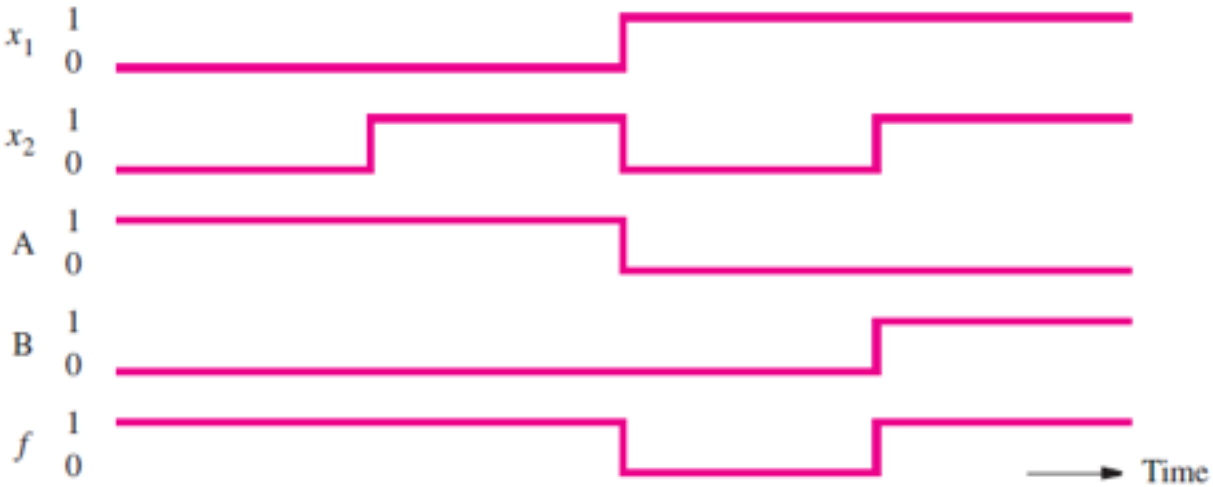


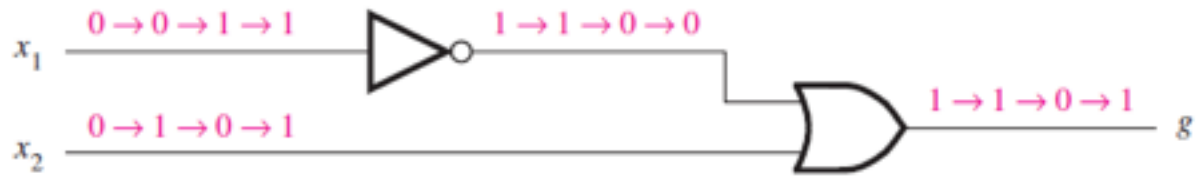
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

x_1	x_2	$f(x_1, x_2)$	A	B
0	0	1	1	0
0	1	1	1	0
1	0	0	0	0
1	1	1	0	1

(b) Truth table



(c) Timing diagram



(d) Network that implements $g = \bar{x}_1 + x_2$

Figure 2.10. An example of logic networks.

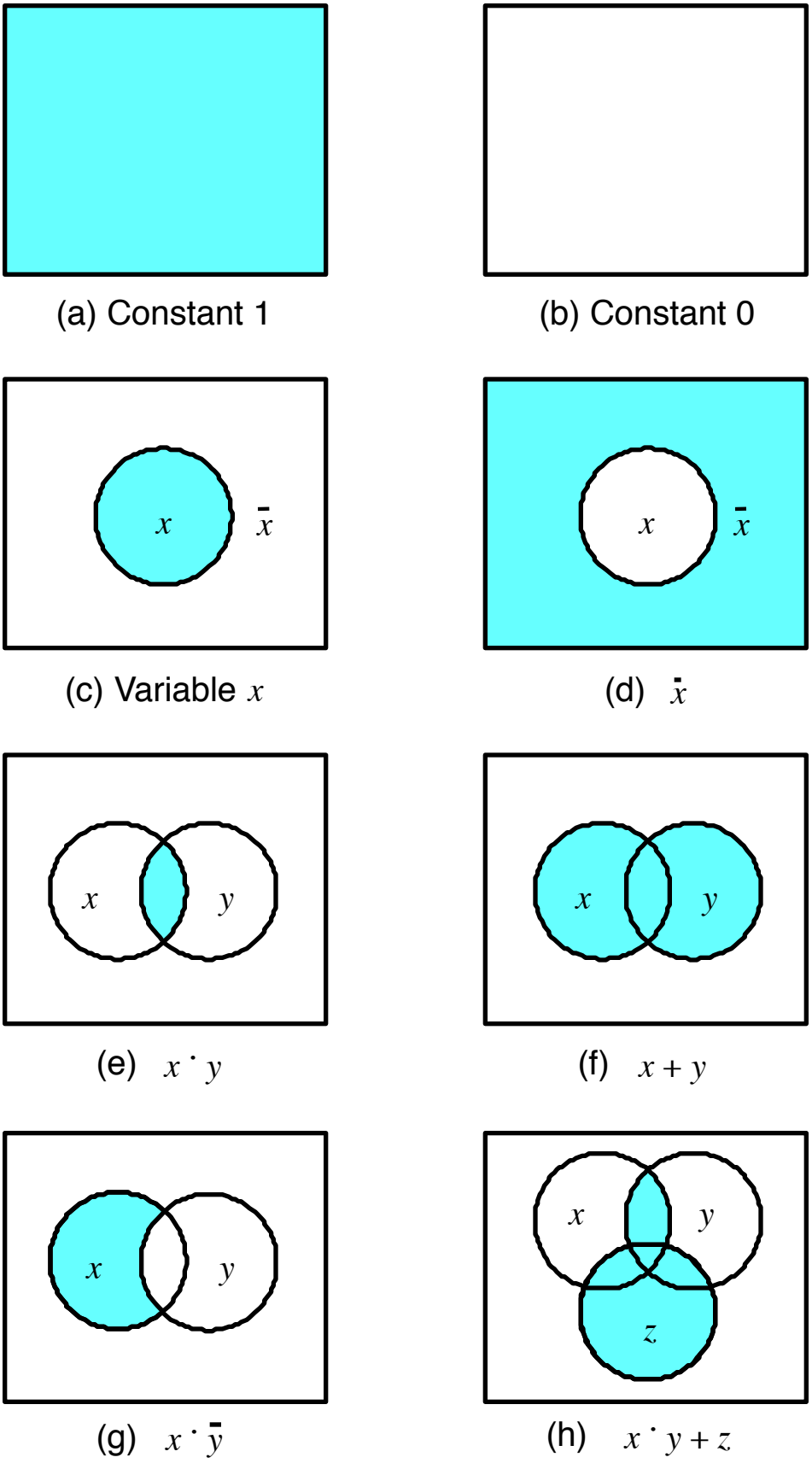
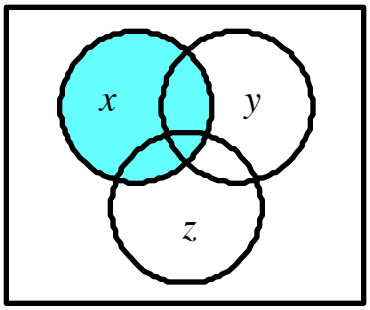
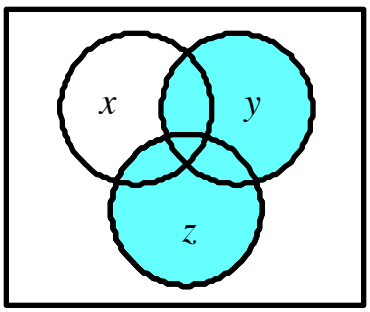


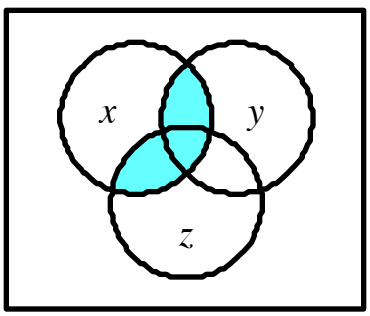
Figure 2.14. The Venn diagram representation.



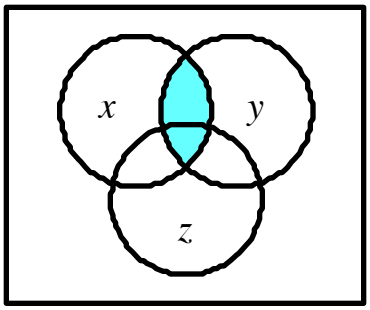
(a) x



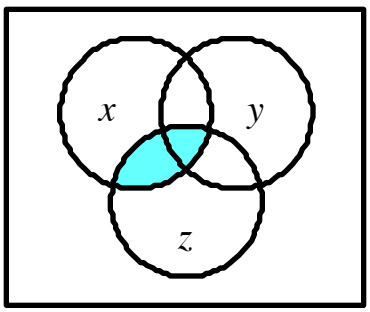
(b) $y + z$



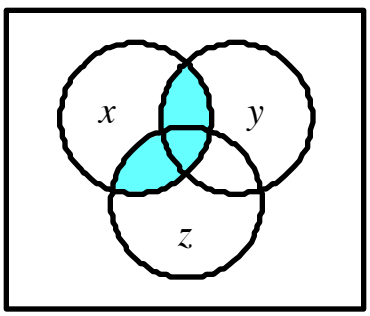
(c) $x \cdot (y + z)$



(d) $x \cdot y$

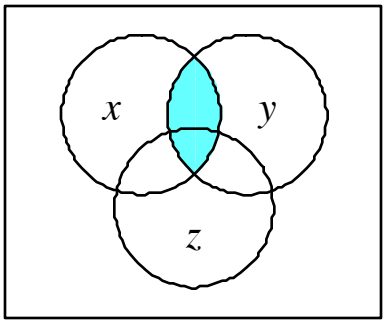


(e) $x \cdot z$

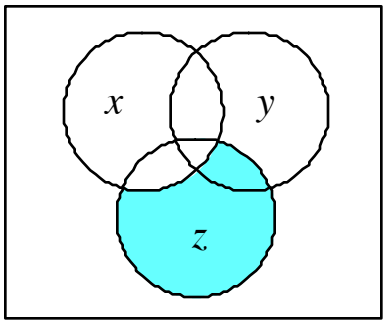


(f) $x \cdot y + x \cdot z$

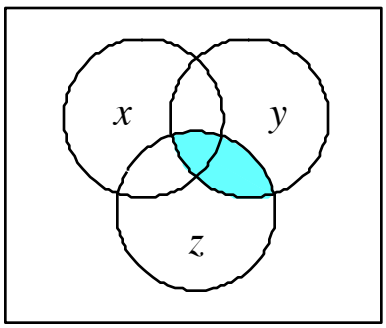
Figure 2.15. Verification of the distributive property $x \quad (y + z) = x \quad y + x \quad z$



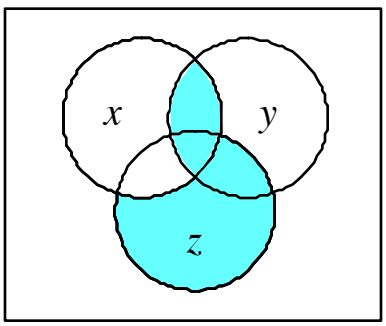
$x \cdot y$



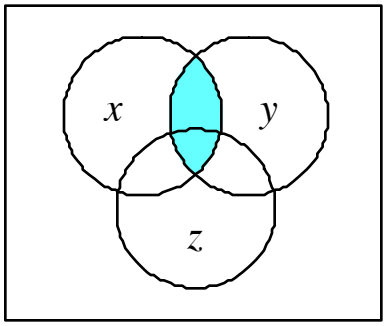
$\bar{x} \cdot z$



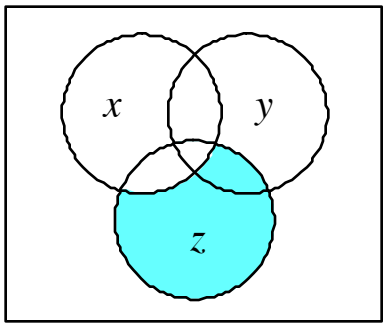
$y \cdot z$



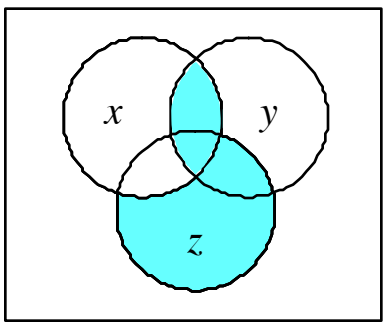
$x \cdot y + \bar{x} \cdot z + y \cdot z$



$x \cdot y$

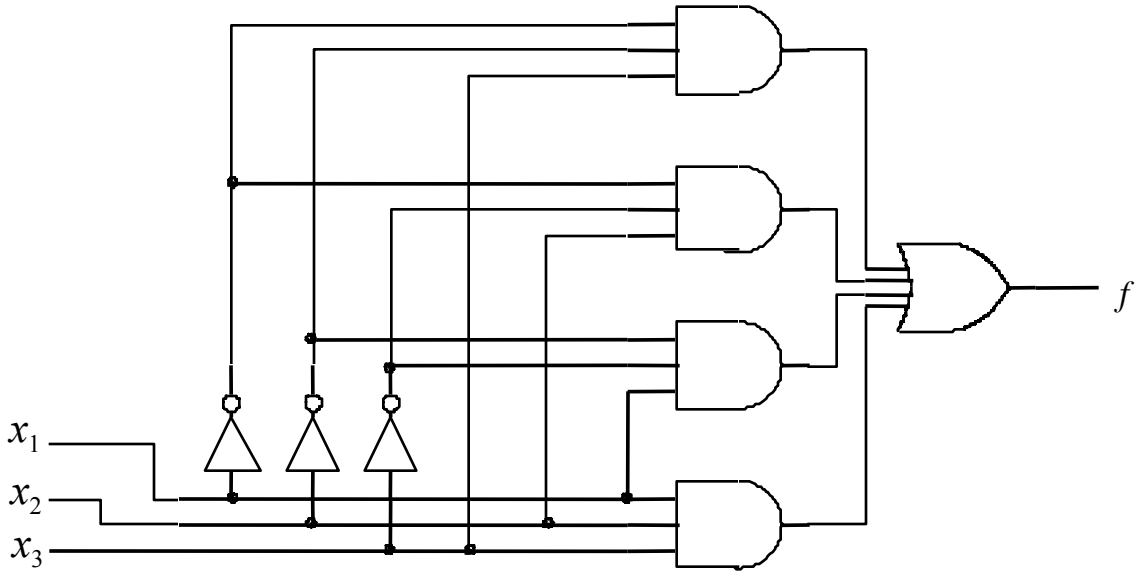


$\bar{x} \cdot z$

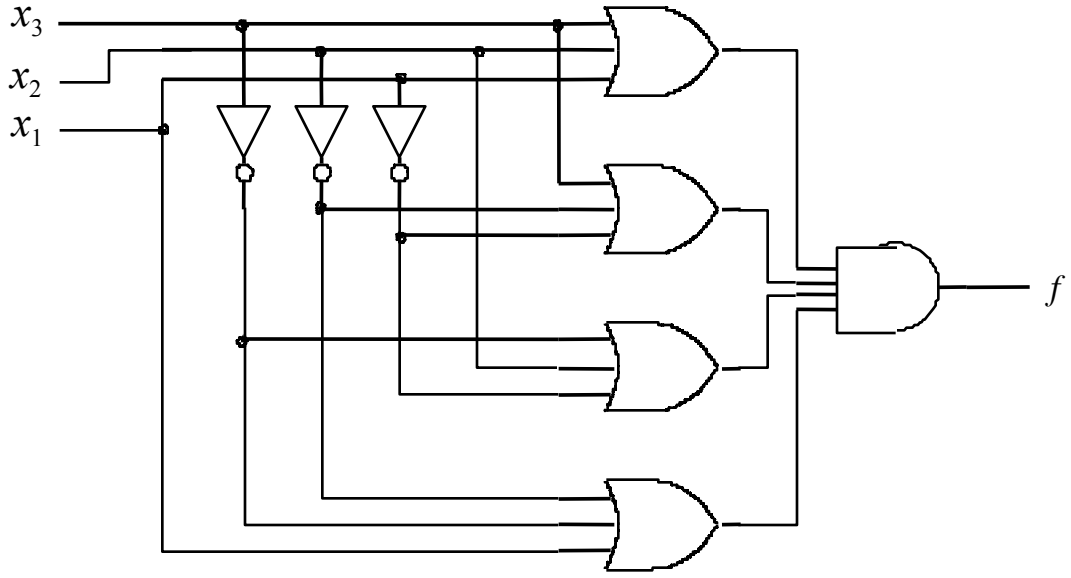


$x \cdot y + \bar{x} \cdot z$

Figure 2.16. Verification of $x \cdot y + \bar{x} \cdot z + y \cdot z = x \cdot y + \bar{x} \cdot z$.



(a) Sum-of-products realization

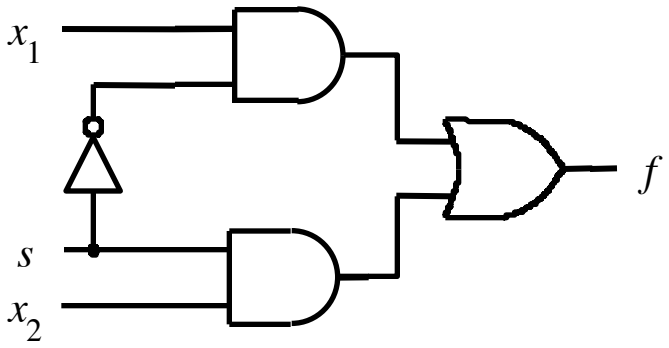


(b) Product-of-sums realization

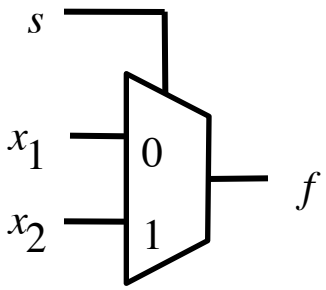
Figure 2.32. Implementation of the function in Figure 2.31.

$s\ x_1\ x_2$	$f(s, x_1, x_2)$
0 0 0	0
0 0 1	0
0 1 0	1
0 1 1	1
1 0 0	0
1 0 1	1
1 1 0	0
1 1 1	1

(a)Truth table



(b) Circuit



(c) Graphical symbol

s	$f(s, x_1, x_2)$
0	x_1
1	x_2

(d) More compact truth-table representation

Figure 2.33. Implementation of a multiplexer.

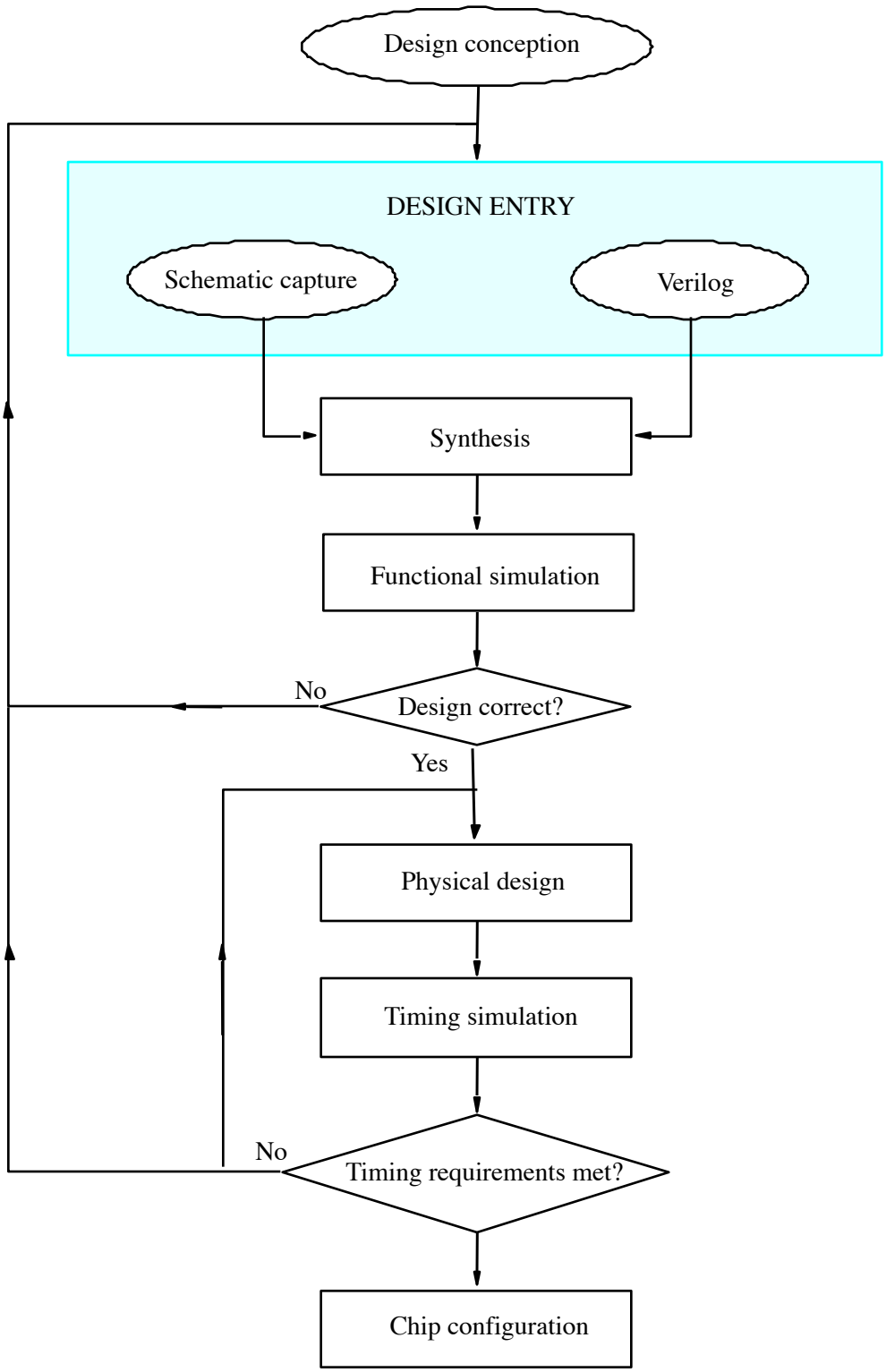
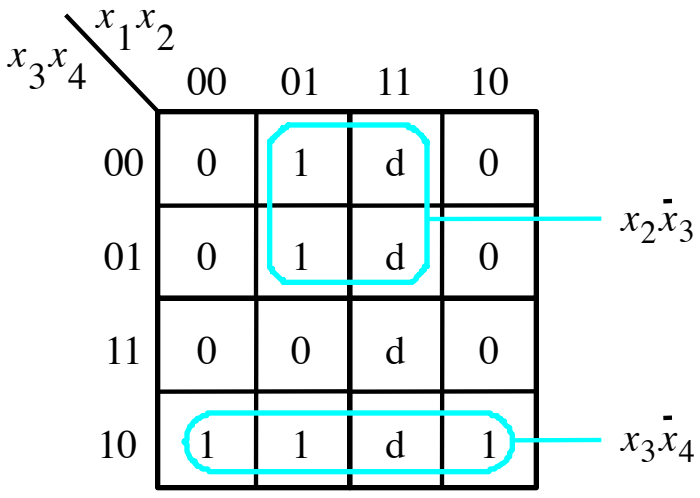
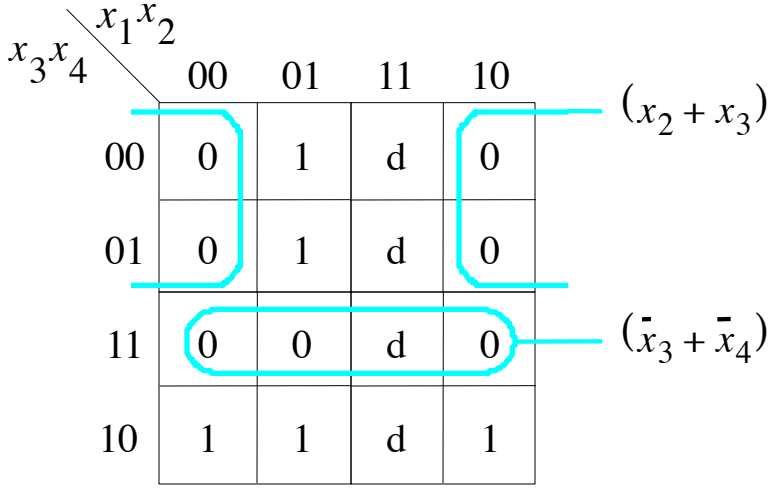


Figure 2.35. A typical CAD system.

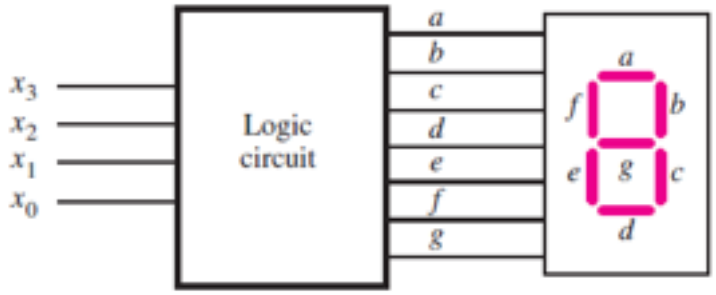


(a) SOP implementation



(b) POS implementation

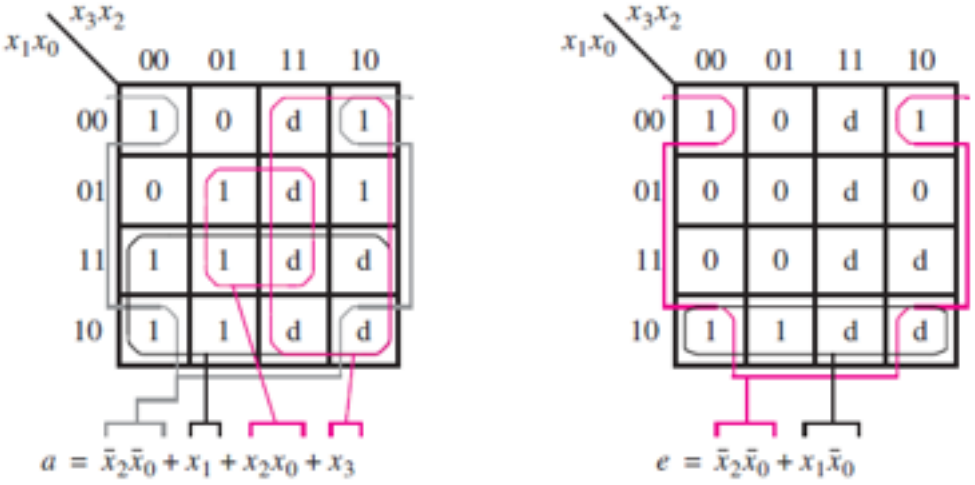
Figure 2.62. Two implementations of the function $f(x_1, \ldots, x_4) = \Sigma\, m(2, 4, 5, 6, 10) + D(12, 13, 14, 15)$.



(a) Logic circuit and 7-segment display

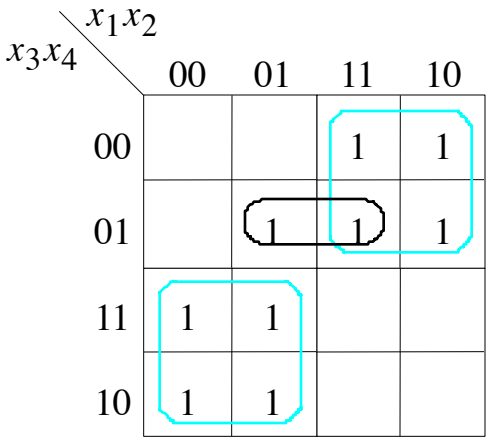
	x_3	x_2	x_1	x_0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

(b) Truth table

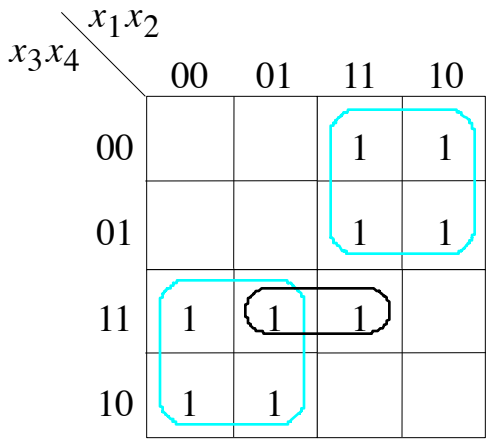


(c) The Karnaugh maps for outputs a and e.

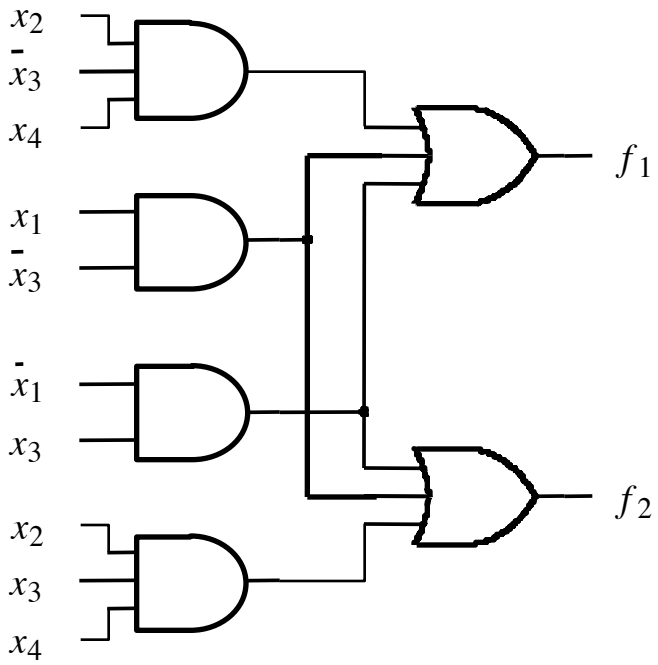
Figure 2.63. Using don't-care minterms when displaying BCD numbers.



(a) Function f_1

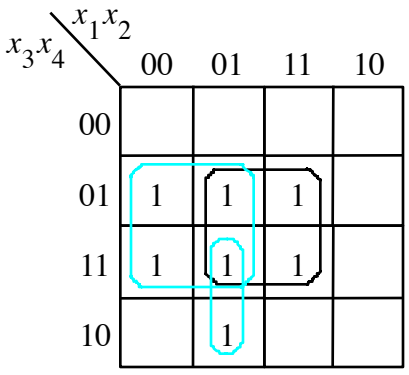


(b) Function f_2

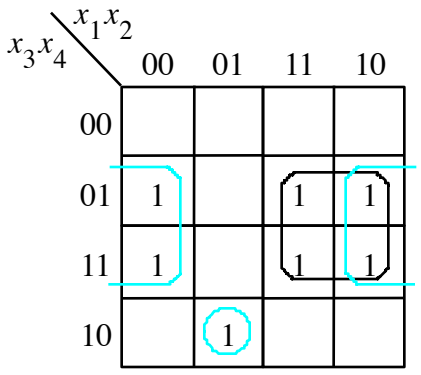


(c) Combined circuit for f_1 and f_2

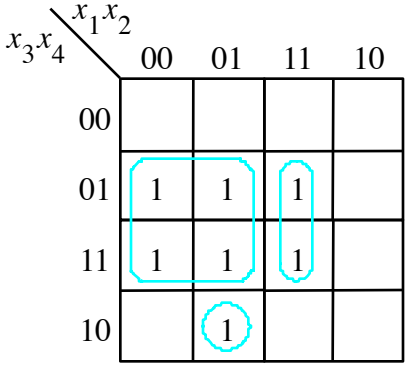
Figure 2.64. An example of multiple-output synthesis.

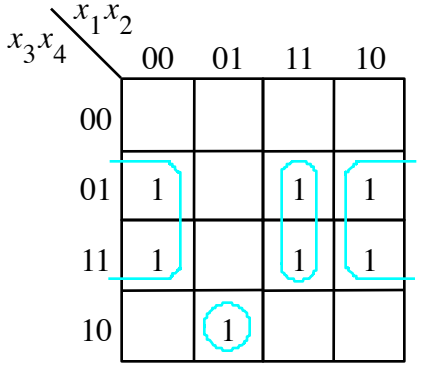


(a) Optimal realization of f_3

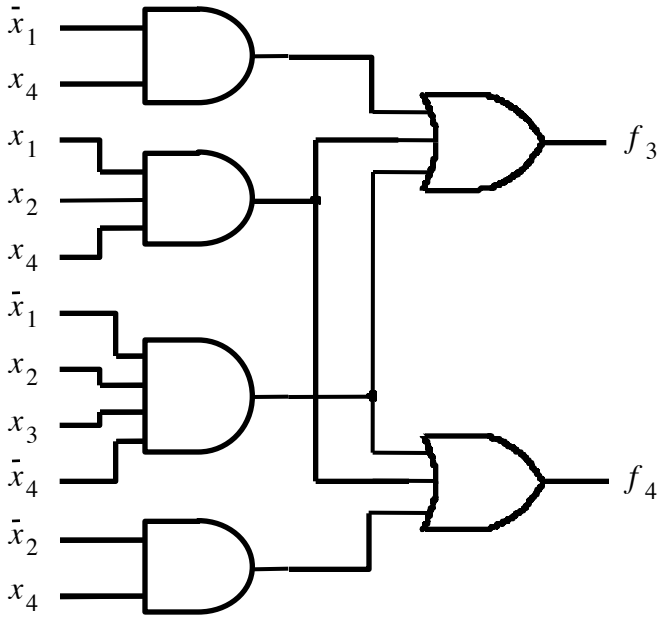


(b) Optimal realization of f_4



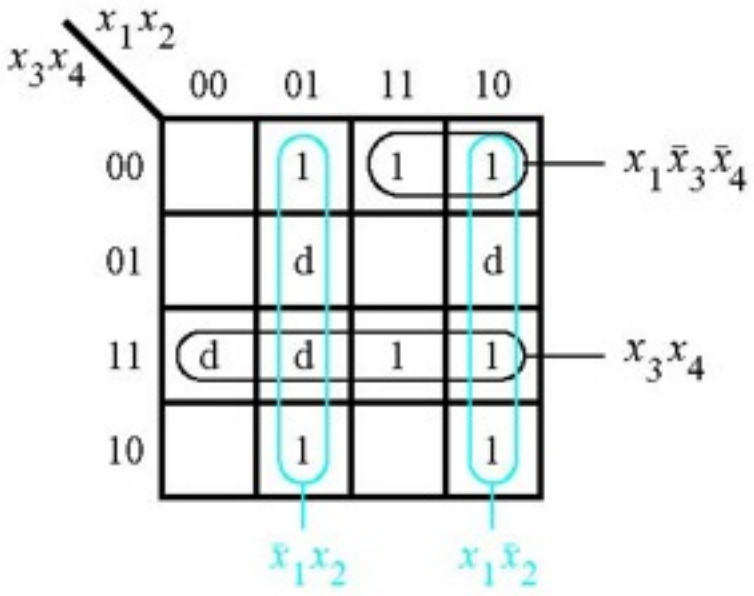


(c) Optimal realization of f_3 and f_4 together

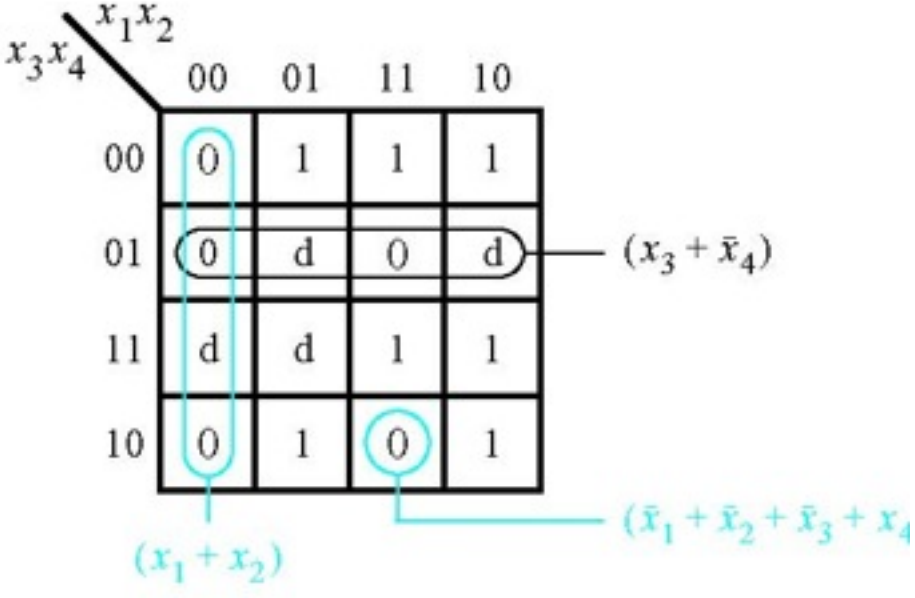


(d) Combined circuit for f_3 and f_4

Figure 2.65. An example of multiple-output synthesis.

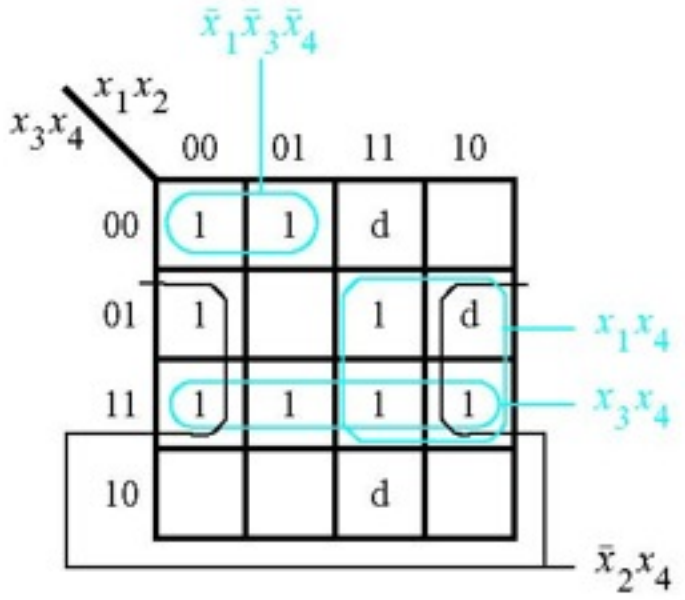


(a) Determination of the SOP expression

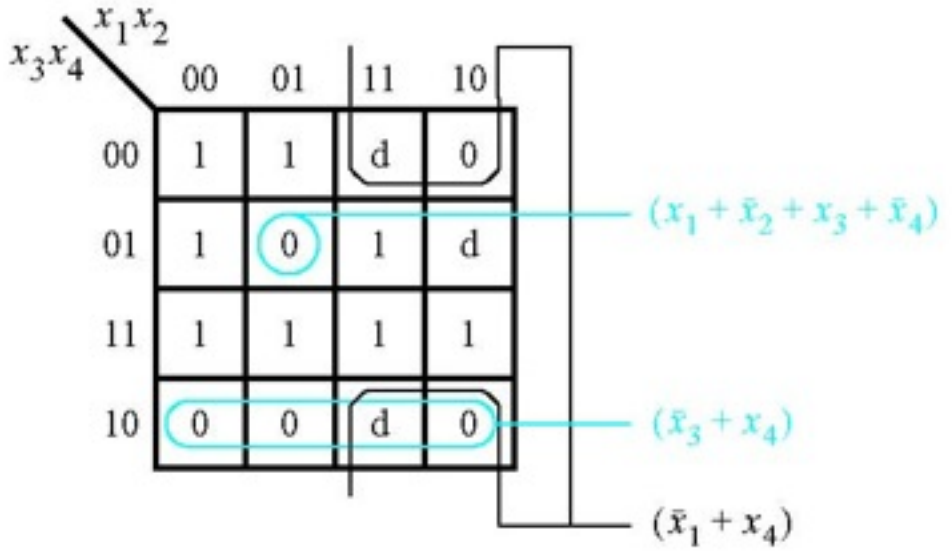


(b) Determination of the POS expression

Figure 2.67. Karnaugh maps for Example 2.26.



(a) Determination of the SOP expression



(b) Determination of the POS expression

Figure 2.68. Karnaugh maps for Example 2.27.

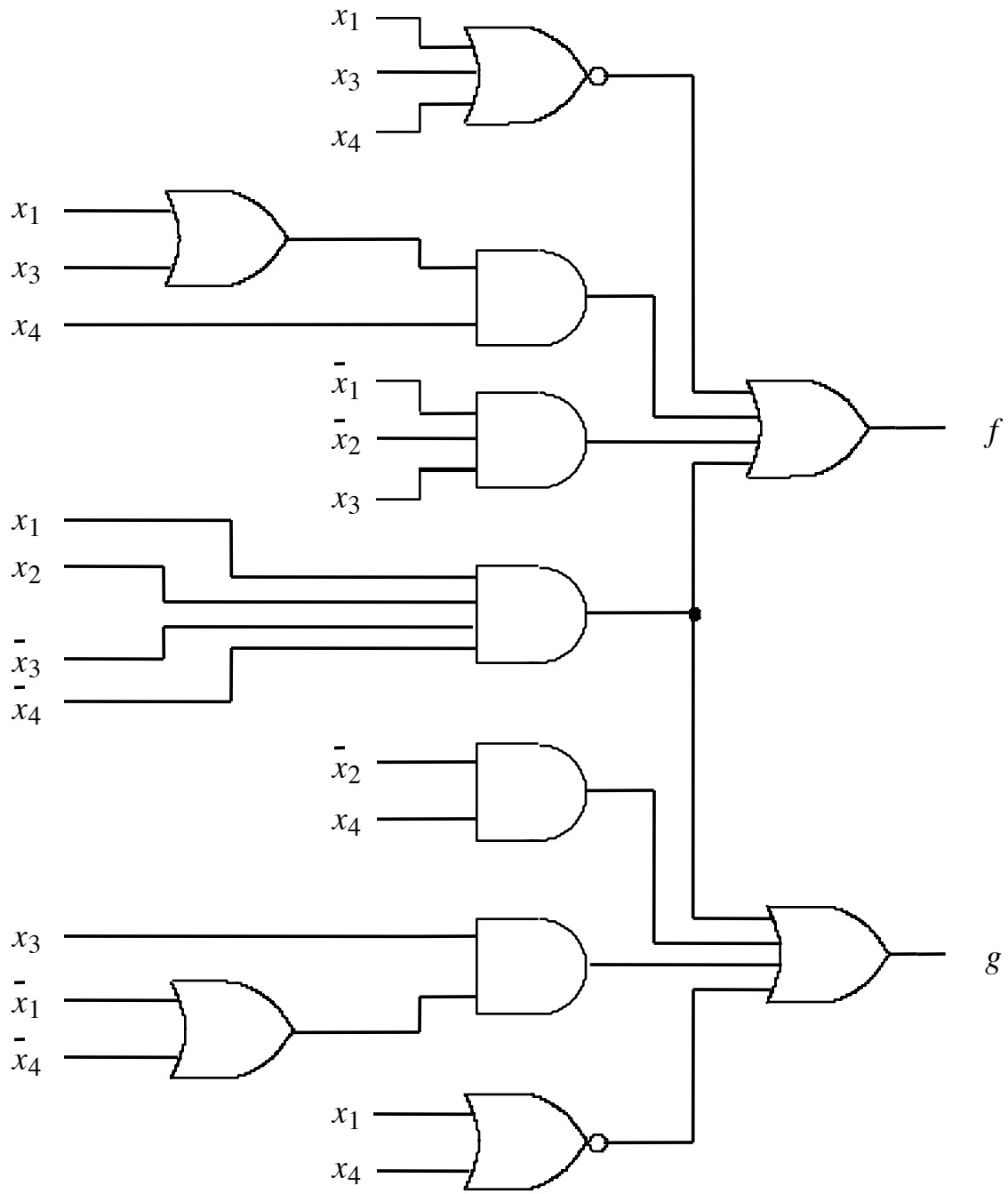


Figure P2.5. Circuit for problem 2.78.

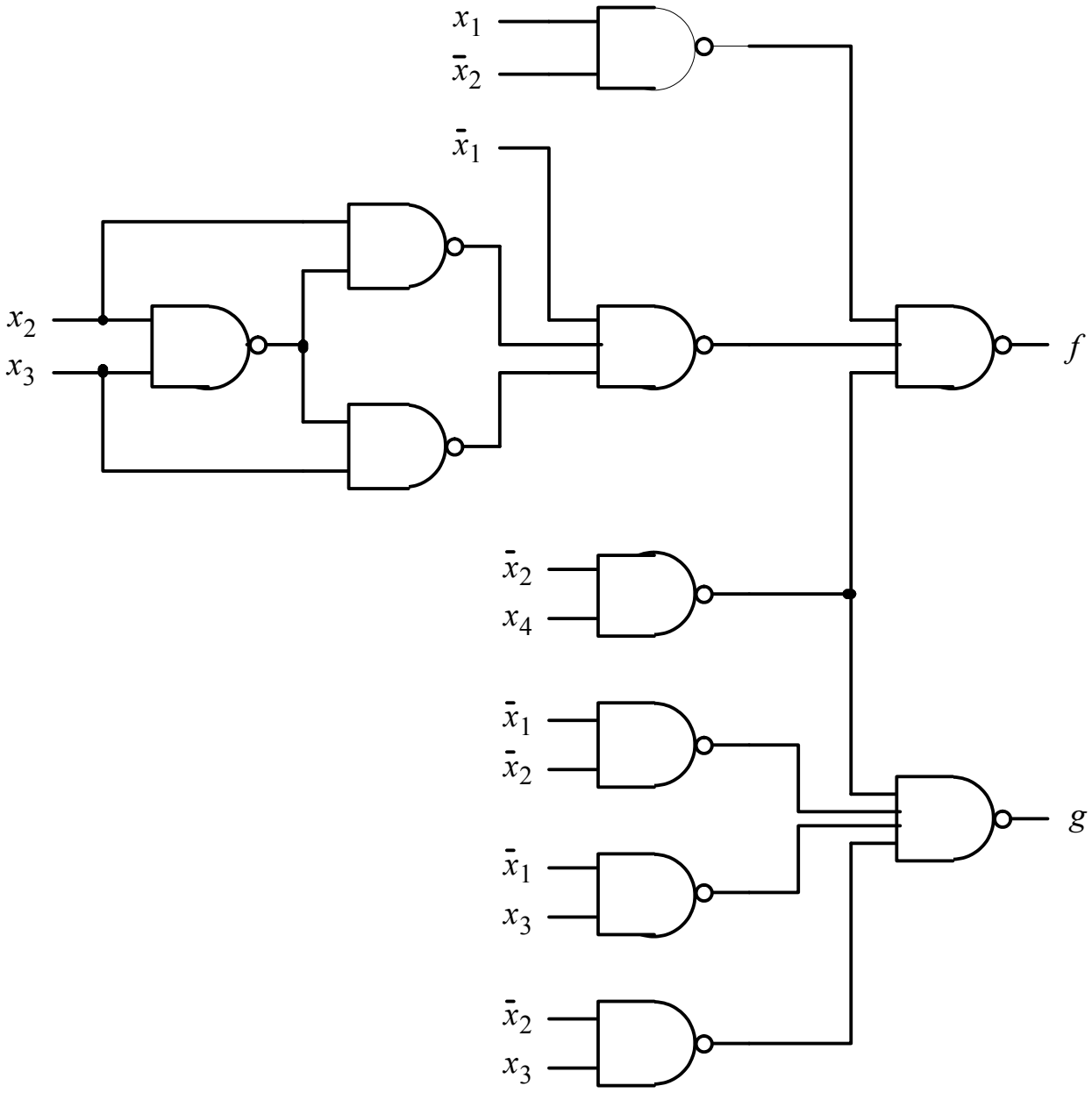


Figure P2.6. Circuit for problem 2.79.