Advanced Phase-Locked Loop

Objectives

The objective of this lab is to refine the design of the loop filter used in the basic PLL lab, and to evaluate the improvements in performance. A second-order filter replaces the first-order filter of the basic PLL lab, and a better phase detector is used. The selection of the filter is an example of control system design with integral action and lead compensation.

Introduction

The basic PLL lab ended with the testing of a basic PLL with first-order filter. While the experiments validated the design, the output signal was found to contain a large amount of ripple. Generally, such a high ripple is intolerable. In most communication systems, the ripple (or harmonic frequency content) of the loop filter output must be attenuated by 50 to 90dB. Unfortunately, the simple RC filter did not provide enough flexibility to improve the design. This lab demonstrates how a more sophisticated loop filter can reduce the output ripple while maintaining good tracking of the incoming signal.

Pre-lab

Show that the loop filter of Fig. 8.28 has transfer function

$$C(s) = \frac{V_{out}(s)}{I(s)} = \frac{k_f(s+b_f)}{s(s+a_f)} \tag{8.31}$$

Give the values of k_f, a_f, and b_f as functions of C_a, C_b, and R_b. Note that the input of the loop filter is a current, rather than a voltage. Accordingly, the output of the phase detector will be a current (the phase detector acts as a current source controlled by the phase error). Such a phase detector is called a *charge pump phase detector*. Assume that the "plant" transfer function is

$$P(s) = \frac{k_{pll}}{s} \tag{8.32}$$

with $k_{pll} = 2.435$ (A/V.s).

The three parameters of the loop filter are k_f, a_f, and b_f . In general, a_f needs to be greater than b_f (this type of control is called *lead compensation*). The locations of a_f and

b_f on the real axis determine the location of the closed-loop poles. We will let $a_f = 8.696\ 10^4$ rad/s, $b_f = 6.25\ 10^3$ rad/s. Plot the root-locus of the PLL system for varying k_f (use the Matlab function *rlocus* to check your results). Note that, for the values of a_f and b_f chosen, the root-locus has two break-away points. Compute the two break-away points, as well as the feedback gain and closed-loop poles associated with the break-away point that is reached first when the feedback gain increases. Deduce what the filter gain k_f should be. Using Matlab, plot the step response of the closed-loop system from the scaled modulating signal x_s to the VCO input signal x_{vco}. Interpret the results. Finally, from the values of k_f, a_f, and b_f , deduce the values of the filter parameters C_a, C_b, and R_b.

Laboratory

Construction and calibration of the charge pump phase detector

EQUIPMENT NEEDED (use a bench having the equipment, if available): oscilloscope, frequency counter, function generator, power supply, and a DMM.
EQUIPMENT TO BE CHECKED OUT: wire kit, two 10x probes, and a Wavetek function generator.
ADDITIONAL PARTS NEEDED: $1k\Omega$, $1k\Omega$ POT (with "tweaker"), 2 - 330Ω, 2 - 470Ω, $0.1\mu F$, 2N3904, 2N3906, 2 – 1N4148.

In this first section of the lab, you will build and calibrate a charge pump circuit to be used with the CD4046 phase detector II (pin 13). The phase detector that was used in the basic PLL lab was an XOR operator. Therefore, if the two signals entering the phase detector were of frequencies separated by $\Delta\omega$, the output was a periodic signal with frequency $\Delta\omega$. If this difference was too large, the PLL's frequency would oscillate and the PLL would not reach

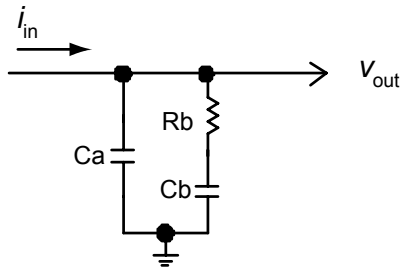

Figure 8.28: A current-to-voltage second-order loop filter

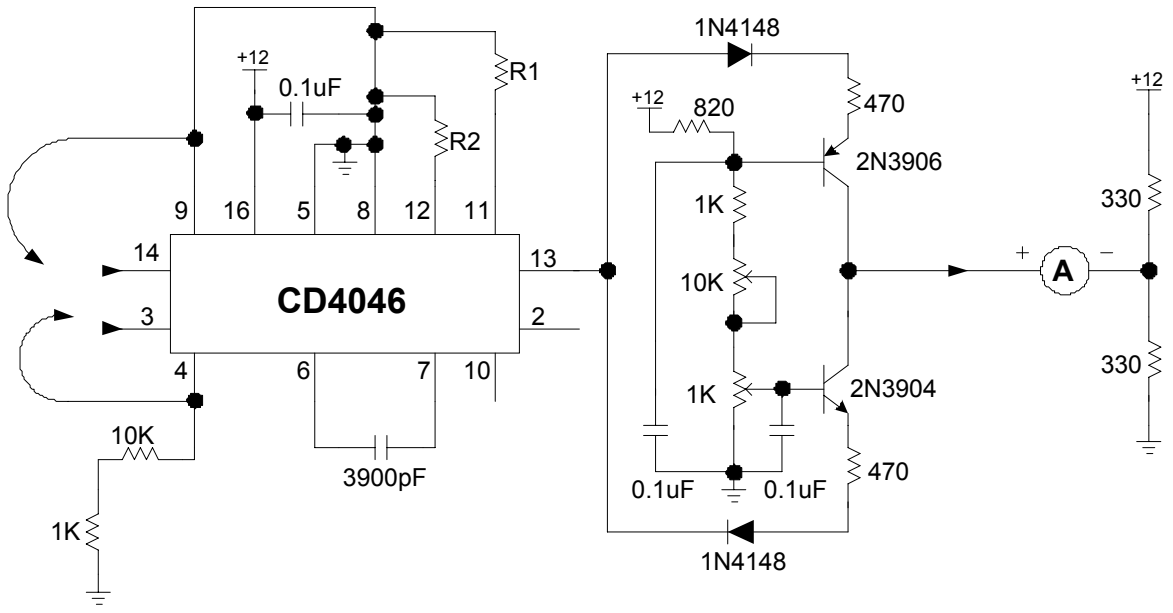

Figure 8.29: PLL with charge pump calibration schematic

lock. Phase detector II is called a phase/frequency detector because it produces an output with positive average value when there is a positive difference between the frequency of the modulated signal and of the PLL. This property improves the ability of the PLL to acquire lock. Another characteristic of phase detector II is that, when the PLL is locked and the center frequency error is zero, the signals are in-phase, rather than in quadrature.

In the CD4046, phase detector II produces pulses whose width is proportional to the phase error. Between the pulses, the output impedance of phase detector II is very high (open). If phase detector II was connected directly to a loop filter input, the resulting PLL system would be severely nonlinear. To ensure linearity, a charge pump conversion circuit must be built and added to the existing PLL circuit. The purpose of the first part of this lab is to build and calibrate the circuit.

The last circuit built in the basic PLL lab should still be assembled. Expand the circuit to build the circuit shown in Fig. 8.29. However, leave pin 13 of the CD4046 disconnected for now. That connection will be made after the transistor circuit is verified. Note that the connections from pin 9 to pin 14 and from pin 4 to pin 3 will change later on.

Double-check your circuit wiring, especially the bipolar transistor circuit. Pay careful attention to the fact that the 820Ω, $1k\Omega$, $10k\Omega$ pot, and $1k\Omega$ pot are in series. Also, double-

check the correct orientation of your transistors and diodes. If you are confident that the circuit is wired correctly, apply power (keeping pin 13 disconnected). The ammeter should read zero. If smoke came from your circuit, replace the bad parts and re-check your circuit. Next, connect the common node between the diodes to +12 volts. Adjust the $10k\Omega$ pot for a reading of $500\mu A$. If you cannot obtain the correct reading, check the top diode and the 2N3906 for proper installation. If $500\mu A$ was obtained, connect the common node between the diodes to ground. Adjust the $1k\Omega$ pot for a –$500\mu A$ reading. If you cannot obtain the correct reading, check the bottom diode and the 2N3904 for proper installation. Once you obtain +/- $500\mu A$ readings, disconnect power.

Connect pin 13 as shown on the diagram. Also connect pin 3 to ground, pin 14 to pin 4 (VCO output), and then re-apply power. Now, adjust the $10k\Omega$ pot for a $+600\mu A$ reading +/- 2%. Then, remove power, connect pin 14 to ground and pin 3 to pin 4, and re-apply power. Adjust the 1kΩ pot for a -$600\mu A$ reading. If successful, the charge pump circuit is now calibrated. The maximum output of the phase detector will be $+600\mu A$ for a $+\pi$ phase shift and a minimum output of -$600\mu A$ for a -π phase shift. Does this correlate with the k_{pll} value used in the pre-lab?

PLL with second-order filter

EQUIPMENT NEEDED (use a bench having the equipment, if available): oscilloscope, frequency counter, function generator, power supply, and a DMM.
EQUIPMENT TO BE CHECKED OUT: wire kit, two 10x probes, and a Wavetek function generator.
ADDITIONAL PARTS NEEDED: two capacitors and a resistor to be determined in the lab.

In this section of the lab, you will use the charge pump circuit (previously calibrated) in conjunction with the current to voltage loop filter shown in Fig. 8.28. Modify your circuit to look like Fig. 8.30. Notice that there are minor wiring changes in addition to the loop filter. In the pre-lab, the values of C_a, C_b, and R_b were computed. Using those values, pick the closest match from the list of choices below.

a) $C_a = 1000$pF, $C_b = 22000$pF, and $R_b = 39k\Omega$
b) $C_a = 390$pF, $C_b = 12000$pF, and $R_b = 27k\Omega$
c) $C_a = 470$pF, $C_b = 15000$pF, and $R_b = 18$k$k\Omega$
d) $C_a = 4700$pF, $C_b = 47000$pF, and $R_b = 5.1k\Omega$
e) $C_a = 1800$pF, $C_b = 6800$pF, and $R_b = 6.8k\Omega$
f) $C_a = 1200$pF, $C_b = 15000$pF, and $R_b = 10k\Omega$
g) $C_a = 2700$pF, $C_b = 18000$pF, and $R_b = 15k\Omega$

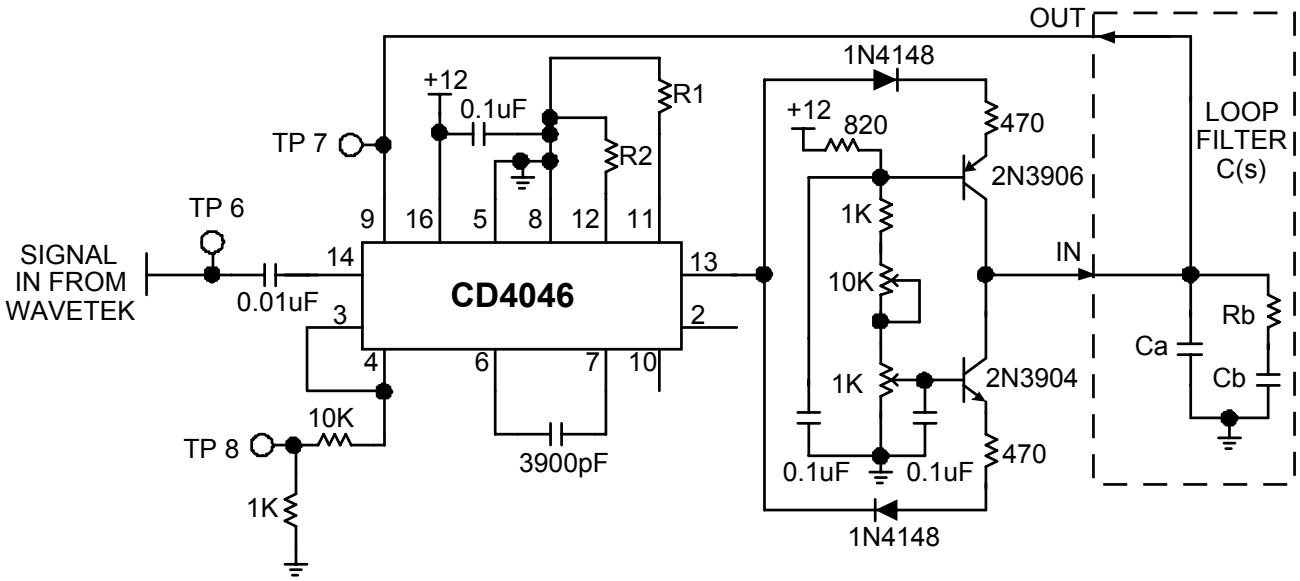

Figure 8.30: PLL with charge pump second-order filter

h) $C_a = 3300$pF, $C_b = 33000$pF, and $R_b = 12k\Omega$.

Verify your choice with the TA and insert the correct C_a, C_b, and R_b in your circuit. Apply power to the circuit and, using the Wavetek, input a 40kHz 8Vp-p sinusoid. Observe the signal input on TP 6 and the VCO signal on TP 8 with the scope triggered from TP 6 (connecting the frequency counter to TP 6 will help to speed-up frequency measurements). The input frequency may need slight adjustment in order to obtain phase lock. Measure and record the PLL hold range and capture range as described in the basic PLL lab. Verify your answers with the TA. Measure the ripple of the VCO control voltage (TP 7). How does this compare with the measurement of ripple in the basic PLL lab?

To observe the PLL step response, the frequency of the Wavetek will be modulated. Set the Wavetek center frequency (frequency knob and vernier) to 40kHz. Next, set up the bench-mounted function generator to modulate the Wavetek frequency. Set the frequency to 200Hz and a square wave output. With the output at minimum, connect it to the VGC input of the Wavetek (lower left connector). Also, using the BNC "T", observe the bench generator output on one channel of the scope while observing TP 7 on the other channel. Trigger from the bench generator (it may be possible to use external triggering on the oscilloscope and trigger from the "sync out" or "TTL out" of the bench generator). Slowly increase the bench generator output. You should notice that the control voltage of the VCO is also a square wave of same

frequency as the bench generator. Characterize the step response. What is the time taken to settle within ±10%? As you increase the output amplitude, how well does the PLL track (observe TP 7)?