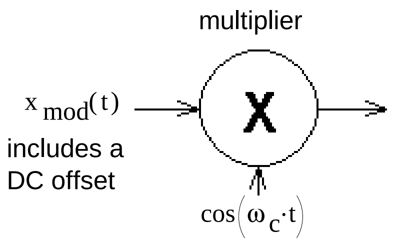
Phase-Locked Loops are a bit of a distraction right here, but we need to cover them for next lab. (6 & 7)

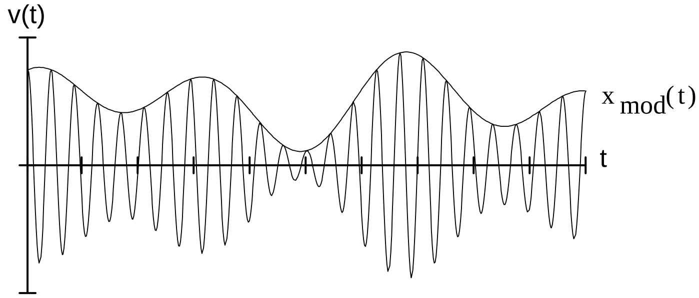
Need parts and breadboard for this lab. PLL IC is expensive and prone to static & handling damage.

See lab 6 handout PAY ATTENTION to warnings in the lab.

Modulation

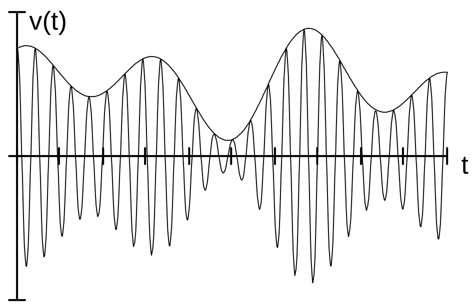
AM = Amplitude Modulation



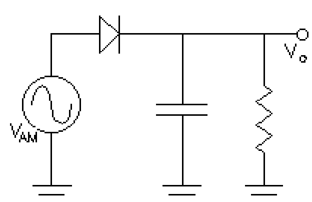


"carrier", ω_c is the "carrier frequency" Simple

Demodulation

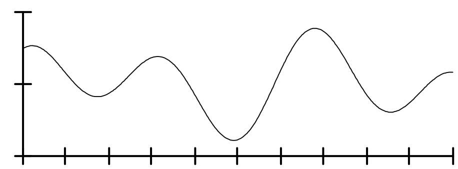


A simple rectifier circuit



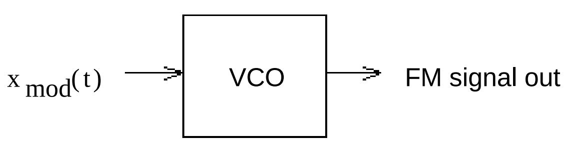
detector

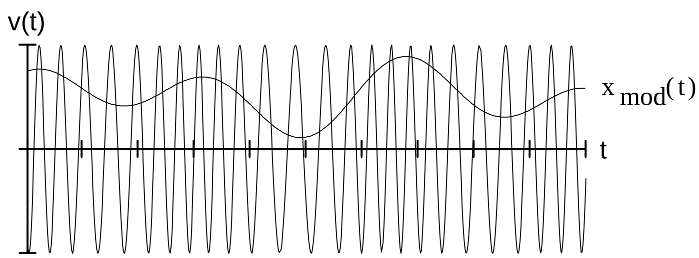
Returns the modulation signal



And a coupling capacitor can remove the DC

FM = Frequency Modulation





Voltage-Controlled Oscillator

ω_c is the carrier frequency and is the output when $x_{mod} = 0$

$\omega_c + k_{vco} \cdot x_{mod}(t)$ is the output frequency

So if: $\cos(\omega_c \cdot t)$ is the carrier, I guess $\cos\left[\left(\omega_c + k_{vco} \cdot x_{mod}(t)\right) \cdot t\right]$ must be the output... WRONG!

actually: $\cos(\theta(t))$

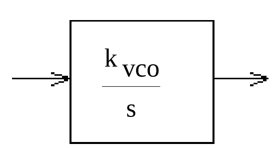
where: $\theta(t) = \int \omega \, dt$ is the REAL relationship between θ and ω

$= \omega \cdot t$ for the unmodulated (steady-state sinusoid) case

so if you want to modulate the frequency:

$$\theta(t) = \int \left(\omega_c + k_{vco} \cdot x_{mod}(t)\right) dt = \omega_c \cdot t + \int k_{vco} \cdot x_{mod}(t)\, dt$$

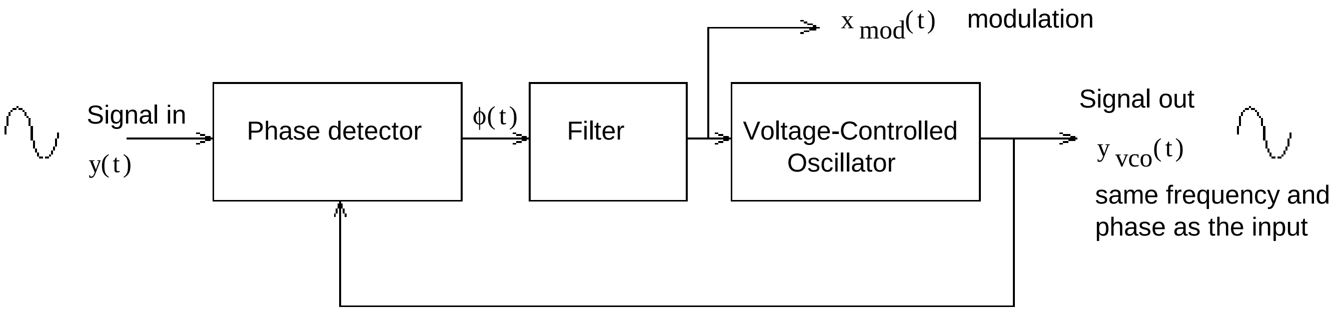
And, the VCO becomes



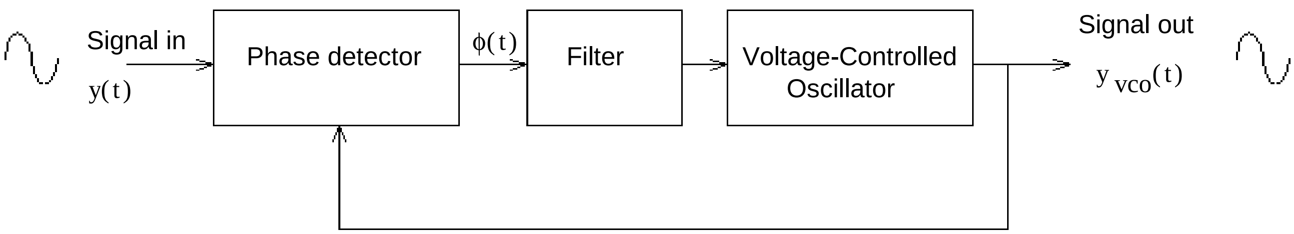
if you just care about $\theta(t)$ and not the carrier

PM = Phase Modulation

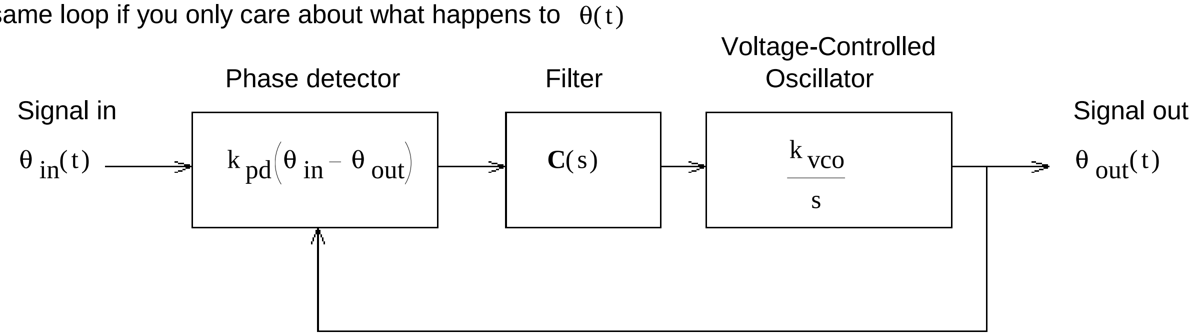
One way to demodulate FM is with a Phase-Locked-Loop.



To analyze the Phase-Locked-Loop (PLL).



The same loop if you only care about what happens to $\theta(t)$

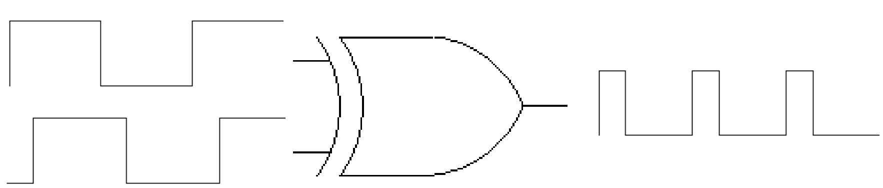


$$\mathbf{G}(s) = k_{pd} \cdot \frac{k_{vco}}{s} \cdot C(s) = \frac{k_{pll}}{s} \cdot C(s) \quad \text{where} \quad k_{pll} = k_{pd} \cdot k_{vco}$$

Closed-loop: $$\mathbf{H}(s) = \frac{\frac{k_{pll}}{s} \cdot C(s)}{1 + \frac{k_{pll}}{s} \cdot C(s)} = \frac{k_{pll} \cdot C(s)}{s + k_{pll} \cdot C(s)}$$

At first glance, that filter, $\mathbf{C}(s)$, doesn't look necessary, but many phase detectors don't put out a nice DC.

Our phase detector in the lab is a good example:



This DEFINITELY has to be filtered

For filter, $\mathbf{C}(s)$, design, see Bodson, section 4.5.4 and PLL labs.

Your challenge in the lab will be to get a good demodulation and a stable system.

PLLs can also be used for frequency synthesis and motor speed control, etc..