University of Utah
Electrical & Computer Engineering Department
ECE 3510 Lab 7
Phase - Locked Loop II

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Note : Bring circuit and lab handout from last week's lab.

Objectives
- Try the other phase detector.
- Experiment with the loop filter used in the basic PLL lab and find the limit of this technique.
- Use the source-follower output and create a second filter just for the demodulated output.
- Use your PLL to create frequency synthesizer

Check out from stockroom:
- Wire kit
- Two 10x scope probes

Parts to bring or buy:
- All parts from last week's Basic PLL lab, built around the CD4046 CMOS PLL IC.
- Two more R_f resistors (same value as the R_f that you used), One $R_f/2$ resistor (half the value of the R_f that you used), 1 kΩ , 1.8 kΩ.
- One more C_f capacitor, 0.01 µF (probably marked 104).

Phase Comparator II
Review last weeks lab and set up the circuit with a simple input obtain a locked output. Your input should be a square-wave between 30 kHz and 50 kHz at about 4 Vpp. Verify that you circuit still works and that it still locks within the full range. Move the filter input from pin 2 to pin 13, so that you are using the second phase comparator. Test the PLL operation again. Pay particular attention to the phase difference between the input and output throughout the range of frequencies. How does this new phase comparator affect the PLL operation?

Place the scope probes on pins 2 & 13 and swing through the range of frequencies. How are these outputs different?

Move the filter input back to pin 2.

Adjusting the Loop Filter
Look back at the last lab and setup function generator to input to the same FM modulation that you used in the very last part of the lab. (38 kHz square-wave modulated with a 200 Hz square wave at 5 kHz deviation.) Look at the demodulated output at the input of the VCO (pin 9). This should be a fuzzy square wave.

Replace R_f in the loop filter with $2R_f$ (2 in series will do). Describe how that changed the time constant of the filter and how that changed the fuzzy square wave output.

Replace C_f in the loop filter with $2C_f$ (2 in parallel will do). Describe how that changed the time constant of the filter and how that changed the fuzzy square wave output.

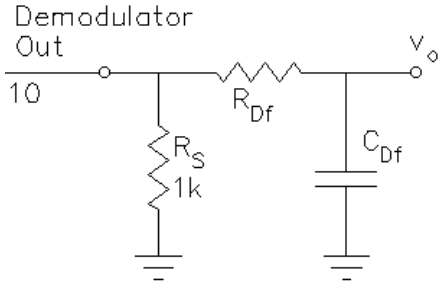
Replace the $2R_f$ in the loop filter with $2.5R_f$ (2 R_fs in series with the $R_f/2$ will do). Describe how that changed the time constant of the filter and how that changed the fuzzy square wave output.

Finally, set the time constant to 6 times the original (Use 3 R_fs). At this point mine was no longer able to demodulate the input. If yours is still working, increase the time constant still further to find the time constant at which the circuit no longer demodulates. What was your maximum working time constant? Return to that circuit. Measure the peak-to-peak ripple, and print the scope screen for your notebook.

What do you think about using a single loop filter to meet the competing goals of system stability and ripple filtering? Restore the loop filter to the original components, and thus the original, stable time constant.

Filter the demodulation separately

Using the loop filter both for system stability and filtering the demodulated output doesn't work very well. The PLL provides another output of the of the demodulation that can be filtered separately, and this strategy will work much better.



First, we need to determine the optimum cutoff frequency (fc) of the new filter. It should filter out the 76 kHz ripple as much as possible and pass the 200 Hz signal as much as possible. But the 200 Hz signal is a square wave with odd harmonics. If we don't pass at least the 5th harmonic, it won't look very good. Find the optimum fc by taking the geometric average of 80 kHz and 5 times 200 Hz. Determine the time constant of the filter from this and select components C_{Df} and R_{df}. Make and connect the filter. Test this new output, measure the peak-to-peak ripple, print the scope screen for your notebook and comment.

Frequency Synthesis Using the Phase-Locked Loop

In this section you're going to see what happens if you add a counter circuit between the VCO output at pin 4 and the phase detector input at pin 3. The output frequency from the counter will be some integer division of the VCO frequency. The input frequency from the function generator will have to be lowered to match. That way you can create an output frequency (in the range of 30kHz to 50kHz) with a lower frequency input from the function generator. The higher frequency signal is said to be "synthesized" from the lower one. If the counter circuit is adjustable, then you may be able to synthesize a range of frequencies from a single input frequency. These synthesized frequencies will all be integer multiples of the input.

Ask your TA to show you the circuit, try a few different divisions and measure the output frequencies. Draw the block diagram of the PLL with the divider and comment on its function in your lab notebook.

Conclusion Check - off and conclude as always. You can now take apart your PLL circuit.