University of Utah
Electrical & Computer Engineering Department
ECE 3510 Lab 6
Basic Phase - Locked Loop

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Note : Bring a breadboard, parts, and lab card this week. You will build a circuit. This Lab Is LONG, do the Pre-Lab *before* coming to lab. Use HP or Agilent 33120 function generator or some instructions won't fit.

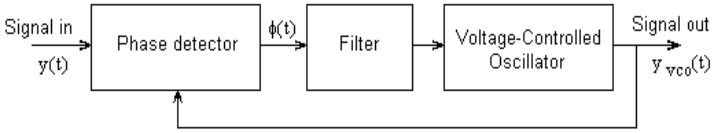
Objectives
- Learn the basic concepts of operation of phase-locked loops (PLL).
- Measure the gain of a voltage-controlled oscillator.
- Construct a PLL with a first-order filter.
- Measure PLL properties such as capture range, hold range, transient response, and steady-state ripple and correlate with analysis results.

Parts to bring or buy:
- Breadboard
- CD4046 CMOS PLL IC
- 1kΩ, 10kΩ, two 18kΩ & a fifth resistor that will be determined in the lab
- 0.1µF, 0.01µF, 3900pF low temperature coefficient capacitor, & a forth capacitor that will be determined in the lab

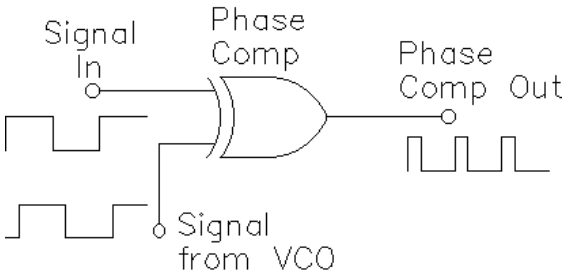
A WORD ABOUT STATIC

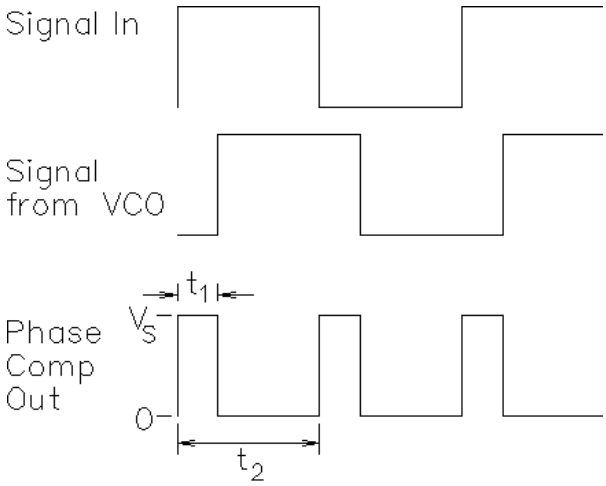
The PLL IC that you will be using is a CMOS part and is static sensitive. Following a few precautions will avoid zapping your IC.
- Ground yourself to your circuit before inserting the IC or working on the circuit. Never assemble or change your circuit with the power applied.
- Connect the ground leads of the power supply and signal source first.
- Apply circuit power first, then signal sources. To change your circuit, remove signal sources first, then power.
- Disconnect signal and power ground leads last.

Introduction
A phase-locked loop (PLL) generates an AC signal whose phase is locked to the phase of an incoming signal. (See section 4.5 in the Bodson text.) It consists of a voltage controlled oscillator (VCO), a phase detector and usually some type of low pass filter. The phase detector compares the output of the VCO to an incoming signal. The result of this comparison is a voltage applied to the VCO, usually through a filter. Phase-locked loops are used for the demodulation of frequency-modulated (FM) signals, for frequency synthesis (creating multiples of a reference frequency), and for other applications.



Pre-lab
The CD4046 phase-locked loop IC contains two different phase detectors. The first one we will use is simply an exclusive or (XOR) logic gate. See the drawing on the next page. It is a good phase detector for square-wave signals, which we will use in this lab. The output of the XOR phase detector switches between 0 and V_s. If the two signals into the XOR have the same frequency and phase (0° phase difference), sketch the output signal. What is the average(V_{avg} or V_{DC}) value of this output? (Yeah, it's just 0V) Repeat for signals that have a $+90^\circ$ phase





$$V_{avg} = \frac{t_1}{t_2} V_S$$

difference (the signal in leads the VCO by 90°).
Repeat once more for +180° phase difference. Find the average (DC) output for negative phase differences. Make sketches if you need to. Plot the average value of the output signal for a phase differences ranging from –180° to 180°. Notice that, within the range 0 →180°, the average value of the output of the phase is a linear function of the phase difference ($\theta - \theta_{vco}$) and can be written as

$$\phi = V_{avg} = k_{pd}(\theta - \theta_{vco})$$

Find the value of k_{pd} in V/rad when $V_s = 12V$. What phase difference produces an average output of $V_s/2$? That's the phase difference that you should see when the PLL is locked at it's mid-range frequency. The frequency range of the VCO, and thus the middle of that range, are determined by components external to the PLL integrated circuit. You will use components that give a frequency range from 30kHz to 50kHz. What phase difference will correspond to a locked PLL output of 40kHz?

Experiment

This lab covers several tasks: 1) Measuring the "gain" (k_{vco}) of the VCO, 2) Constructing the PLL circuit around the CD4046 IC and 3) Designing a first-order filter for the PLL. Note: Sections of this lab and of the next lab use the same or very similar circuits. Therefore, don't prematurely disassemble any circuits.

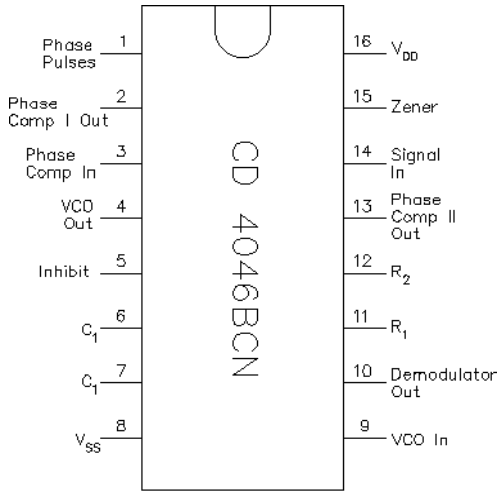
To insure repeatability in the experiments, the 3900pF capacitor in this lab should be a low temperature coefficient type. The small epoxy coated, shiny, smooth, brown capacitors with a 392G printed on them should work fine. Do not use the bigger, dull, brown rectangular or disc-shaped capacitors. (The 392 reads like a resistor code 39 x 10^2 pF.)

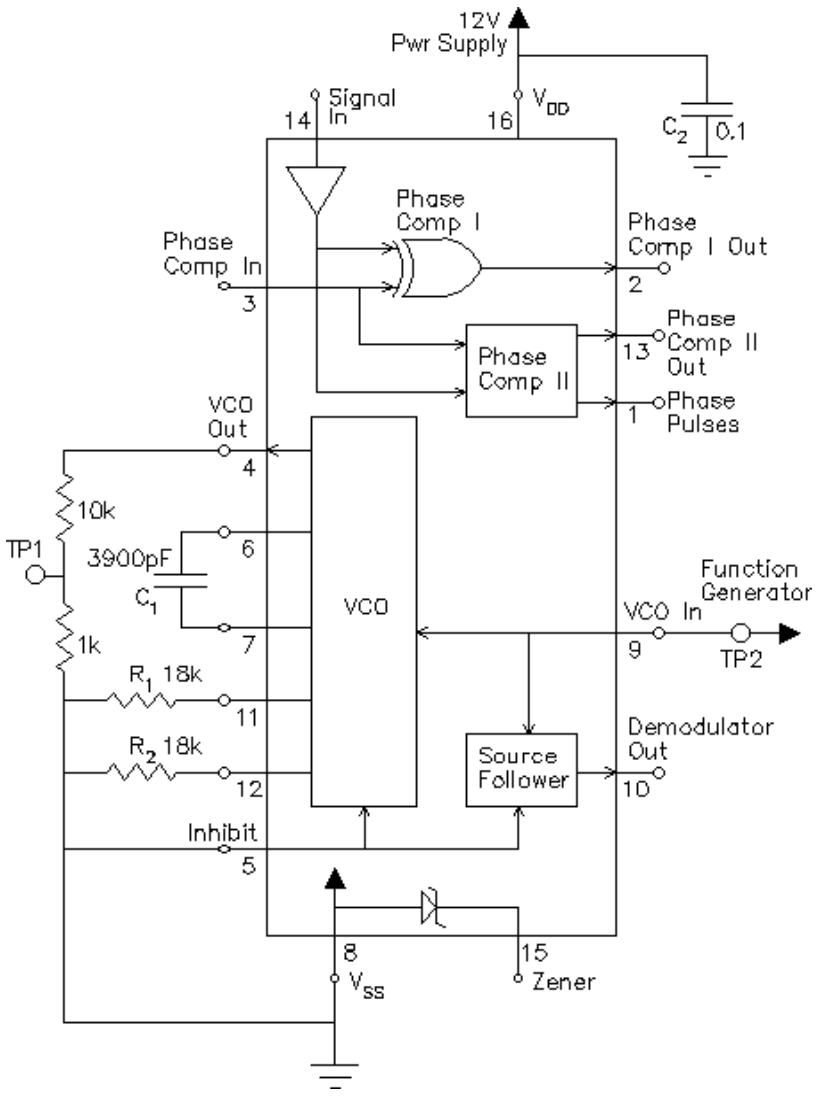
Measuring k_{vco}

Begin by calibrating the 10x probes to your oscilloscope. If you are unsure of how to do this, see the box on the last page (the back) of this lab.

The purpose of a Voltage-Controlled Oscillator (VCO) is to produce a signal (square wave in this case) whose frequency is proportional to its input voltage. The objective of this section of the lab is to find the constant of proportionality (k_{vco}).
Where f_0 is the free-running frequency of about 30kHz.

$$f_{vco} = k_{vco} V_{vco} in + f_0$$





Assemble the circuit shown at right on a breadboard.

Everything drawn inside the big box is inside the CD4046 PLL IC. The numbers around the box are the IC pin numbers. Notice that there are a number pins that we don't use. They are all output pins, so they can all be left disconnected. Be sure to keep the 3900pF capacitor (C_1) as close to the PLL IC as possible.

The data sheet for the CD4046 indicates that with R_1 = 18kΩ , R_2 = 18kΩ, C_1 = 3900pF and V_{DD} = 12V (V_{DD} = V_S) the VCO frequency range will be 30kHz to 50kHz.

When you've built the circuit, connect a digital multimeter (DMM) to TP 2 (pin 9). Connect the power supply to ground (-) and V_{DD} (+). Turn it on, and adjust it to 12V.

Turn on the function generator. Push and hold the DC offset until it displays DCV. It is now set to output DC only (twice the volts shown on the display). Connect it to ground and TP2. Connect the scope to ground and TP 1 so you can observe the output of the VCO and measure the frequency of that output.

Adjust the VCO control voltage by adjusting the function generator DC offset voltage **(POSITIVE voltages ONLY, a negative voltage may damage the PLL)**. Make a table of frequencies for a number of voltages. Expect it to be nonlinear below about 1V, so take a few readings there. It will also be nonlinear above about 10V, in fact will nearly flatten out. The function generator won't give you a voltage above 10V, so, to see this effect, temporarily lower the supply voltage to 10V and see what happens in the 8 to 10V VCO input range. Return V_S to 12V. Make a plot of frequency vs. voltage. Assume the plot is flat above 10V.

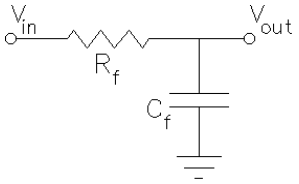
Determine the range of control voltage that results in a linear VCO frequency response. Determine the "gain" of the VCO, or k_{vco} (in Hz/V), in that linear range. Deduce the value of the Phase-Locked Loop gain ($k_{pll} = 2\pi k_{vco} k_{pd}$) using the value of k_{pd} determined in the pre-lab. ($k_{pll} \approx$ 50k.) Note that the transfer function from the VCO input to the output of the phase detector is then

$$P(s) = \frac{k_{pll}}{s}$$ and constitutes the "plant" to be controlled.

Turn off the function generator and then turn off the output of the power supply.

Basic PLL

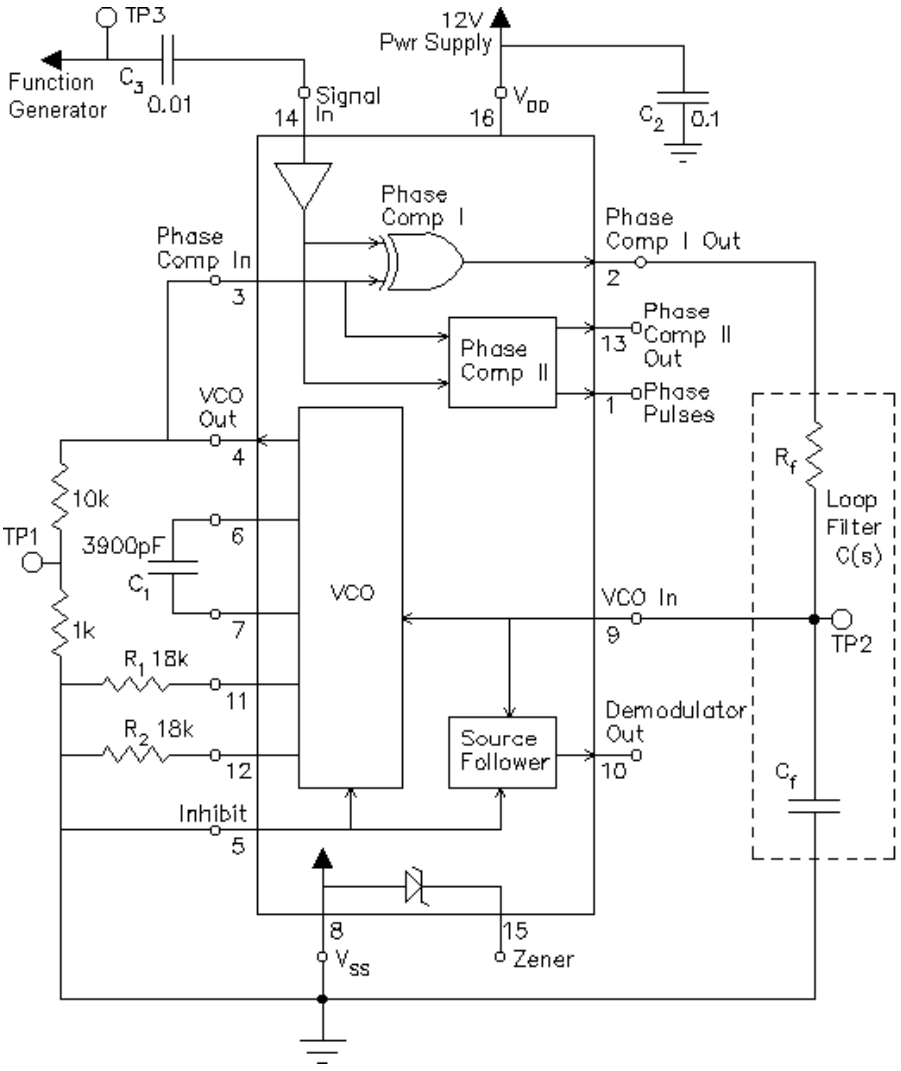
In this section, you will build a complete PLL circuit and measure its characteristics. It will include a first-order low-pass filter between the output of the phase detector and the input of the VCO. R_f and C_f together make make that simple RC filter.



Considering the circuit above, show that the transfer function of the loop filter (which takes the role of the compensator, C(s)) can be expressed in the form

$$C(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{kf}{s + af}$$

Show that k_f and a_f both equal $1/R_fC_f$ (they turn out to be the same).



Find $G(s) = C(s)P(s)$ and the closed-loop transfer function, call it $H(s)$ or $T(s)$.

Show that to get a desired damping factor of $\zeta = 0.707$ (see section 4.5.4 in the text), we need

$$af^2 = 2k_{pll}kf$$

Using the value of k_{pll} determined in the previous section, determine the required product of R_f and C_f ($\approx 10^{-5}$). Now, to find values for the two components, you arbitrarily select one, and then calculate the other. From the list of standard values below (all in pF), select a C_f

(possibly one you already have):

390, 470, 560, 680, 820, 1000, 1200, 1500, 1800, 2200, 3300, 3900, 4700pF

Given this value of C_f, determine R_f and see if it is close to a standard value between 10kΩ and 100kΩ. If not, try a different capacitor value. When you have values you like, construct the full circuit.

Test the PLL

Apply power, turn on the function generator, set it to 40kHz, 8 volts p-p square wave (shows 4 Vpp), and connect it to the circuit through the coupling capacitor, C_3. With the scope, observe the signal input at TP 3 and the VCO output at TP 1. Trigger the scope on TP 3. With this set-up, the two waveforms on the scope should appear "in sync." In other words, the VCO output waveform should be stationary and at the same frequency as the input waveform (the PLL is locked). If not, double-check your PLL circuit (see common errors on the back page of this lab). Check the R_f and C_f values. If your scope only has 2 channels, print a copy of the scope screen for your notebook.

Connect the DMM (set to DC) to TP 2 (pin 9), the VCO control voltage input. Slowly decrease the input frequency. Note that the VCO control voltage decreases as well. As you drop below 30kHz or so, you should notice that the VCO signal looses sync with the input signal. In your lab notebook, explain why the PLL looses sync. (You can understand why if you remember how the VCO works from the first section of this lab and if you watch the DMM.) See if the PLL can loose sync if you adjust the input frequency too high (above about 50kHz). Between the limits you just found (~30kHz and ~50kHz), the VCO frequency should track the input frequency, does it do so? In the next paragraph you'll explore these limits in more detail.

Measure the PLL's hold range and capture range

The hold range is the range of input frequencies for which the PLL maintains phase lock. The capture range is the range for which the PLL acquires phase lock. To measure the lower edge of the hold range, start the input frequency at a point where the PLL is phase-locked, then reduce the input frequency until the PLL looses lock. The lowest frequency where lock can be maintained is the lower edge of the hold range. To measure the lower edge of the capture range, start the input frequency at a point where the PLL is not phase-locked, and raise the frequency until the PLL acquires phase lock. That frequency is the lower edge of the capture range. These two will be very close (if not the same). You will probably have to go in and out of lock a number of times at ever smaller frequency steps to find the lower edges to the nearest 10Hz. Find the upper edges the same way. Adjust the input frequency into the lock range.

A QUICK REVIEW OF OSCILLOSCOPE PHASE MEASUREMENT

To measure phase on the oscilloscope, simply measure the time between two similar points on two waveforms. Divide the time measured by the signal period and multiply by 360 degrees to give the phase difference in degrees.

The Agilent scopes will perform this measurement for you if you push Quick Meas, Select Phase, Measure Phase and select the source you're **not** triggering on. Other digital scopes should be similar.

Accurate phase measurements require properly compensated probes.

Plot the phase difference vs. frequency
On the scope you should see two square waves, somewhat out-of-phase. In this section you'll vary the input frequency through the hold range and plot that phase difference vs. frequency. You only need to measure 4 or 5 frequency points, see the box for details of how to make the phase measurement. Does the phase remain constant over the input frequency range? Can you explain why not?

Observe the VCO input
Set the input frequency to 40kHz and measure the VCO control voltage input (TP 2 (pin 9)) with the scope. Is this control voltage a nice clean DC voltage? If not, how much ripple is present? What is the source of the ripple? Hint: use the other channel of the scope to observe pin 2 on the PLL and remember the time constant of the loop filter. Print a copy of the scope screen for your notebook. Note: If you are using a 4-channel scope, and can display pin 2 and all 3 test points (TP 1, TP 2, & TP 3) on the screen at once, then this one print will do for be sufficient for both this and the print asked for earlier.

In theory, the ripple could be decreased by lowering the bandwidth of the loop filter. However, the constants k_f and a_f cannot be set independently. To find out what would happen if the bandwidth of the RC filter was decreased, sketch the root-locus of the closed-loop poles as a function of a_f ($a_f = 1/(R_f.C_f)$). That is, as though a_f were the "gain". The closed loop poles are the poles of the closed-loop transfer function you found earlier and thus the roots of

$$s^2 + a_f(s + k_{pll}) = 0$$

Notice that if the a_f factor were the "gain" (like k) of a normal root-locus, then the corresponding open loop transfer function would be

$$G(s) = \frac{s + k_{pll}}{s^2}$$

This is an example of an unconventional root locus discussed in class and covered in homework RL8. Draw this root locus. Find the current closed-loop pole locations on this root locus. Explain, using your new root locus plot, why increasing the time constant of the loop filter (decreasing a_f) is not desirable. Refer to p. 51 in the text and think in terms of a/b as the a_f term is decreased. If you want to, you can try to add a resistor in series with R_f and/or a capacitor in parallel with C_f to increase the time constant a little. See if the system still locks. If it does, set that extra resistor or capacitor aside for now and you can try it again later with the square-wave FM.

Frequency Modulate the input
Next, the input frequency will be modulated, first by a sine wave and then by a square wave to view the PLL step response. Set-up the function generator as shown below.

Buttons	Display			
Shift-FM (⊓)	1.000 kHz	adjust to:	38.00 kHz	
Shift-Freq	10.00 Hz	adjust to:	200.0 Hz	(Adjusts modulation frequency)
Shift-Level (Ampl)	DEVIATION			
Quicky changes to:	100.0 Hz	adjust to:	5.000 kHz	(Adjusts modulation frequency amplitude)

Observe TP 2 (pin 9) on the scope. Run a BNC to BNC cable from the SYNC output of the function generator to other channel of the scope and trigger on this channel. (I had to adjust the trigger level to get a stable trace.) The fuzzy sine wave is the demodulated output signal. A cleaner version can be found on pin 10, but if you observe that, be sure to return the scope to TP 2 (pin 9) before you go on. As always, comment in your notebook about what you did and what you found. Next you'll change the modulation to a square wave.

Set-up the function generator as shown below.

Buttons	Display	
Shift-Menu	A:MOD MENU	
v (down-arrow)	1:AM SHAPE	
>, > (Or turn knob)	3:FM SHAPE	
v	SINE	
> (Or turn knob)	SQUARE	(Adjusts modulation shape to a square wave)
Enter	ENTERED	

TP 2 (pin 9) should now have about a 5 volt p-p square(ish) wave. Describe the response of the VCO control voltage (TP 2 (pin 9)) in terms of speed of response, overshoot and noise (ripple). Print a copy of the scope screen for your notebook. If you found a longer time constant filter in the last section that worked, try that again here. (You may have to lower the deviation to keep things working.) Note the overshoot now. Print a copy of the scope screen again if you have something interesting. Return the circuit to what it was.

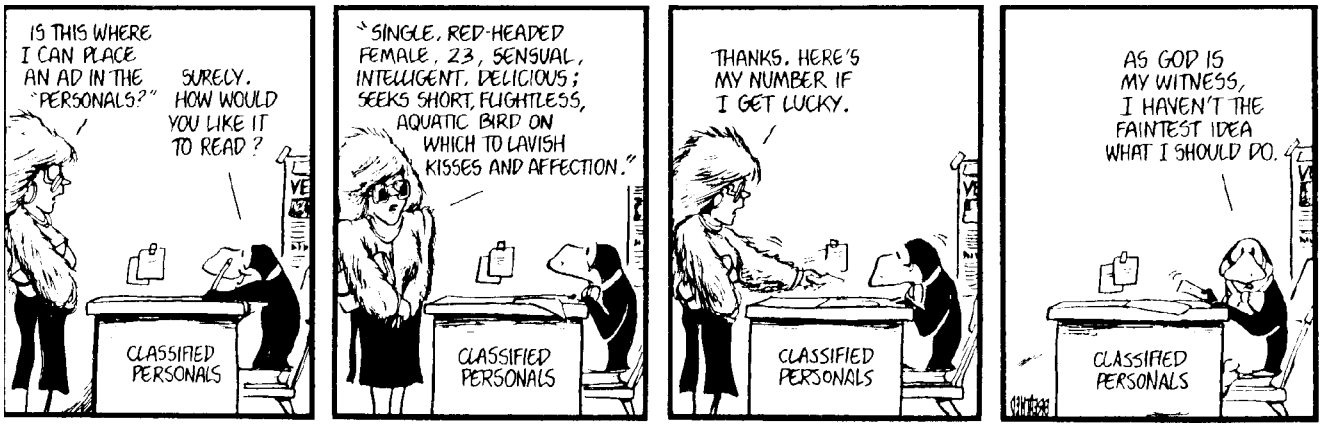
Slowly increase the modulation (deviation) as shown below:

Buttons	Display	
Shift-Level (Ampl)	DEVIATION	
Quicky changes to:	5.000 kHz	slowly adjust up

If you adjust the deviation too high, the output frequency will shift beyond the hold range of the PLL and you'll see some interesting effects.

Breath a sigh of relief, the lab is finally over.

Conclusion Check - off and conclude as always. Do not take apart your PLL circuit. Most of it will be used next week in the advanced PLL lab.



Scope Probes & 10x Probe Compensation

In this lab you may want to use 10x scope probes instead of the BNC-to-clip cables (1x) that you used last time. The 10x refers to the fact that the input impedance to the scope is 10 times higher when you use a 10x scope probe. When you hook the scope directly to your circuit, the circuit "sees" a load of 1 MΩ in parallel with about 13 pF. When you use a 10x probe, the circuit will instead "see" a load of 10 MΩ in parallel with about 1.3 pF. This lessens the effect of the scope on the circuit, making your measurement more accurate. The price of this higher impedance is that the scope will only get one tenth the signal that it would with a 1x probe. You need to be aware of these tradeoffs in scope performance to get the most accurate measurements from the scope.

There is , however, one little "gotcha" with 10x probes. Notice that I said that the scope input capacitance was "about" 13 pF? Well, each scope is a little different and the scope probe will need to be adjusted or "compensated" each time it is used with a different scope, this is especially true in our lab, where the same probes are used with the Tektronics, Agilent, & HP scopes. The frequency response of an uncompensated probe can seriously mess-up your measurements, especially of frequency response and phase. You should always compensate a 10x probe before using it.

To compensate a probe:

1) Connect it to the scope as normal.
2) Switch it to 10x if it has a switch.
3) Determine how to adjust your probe. Most probes have a small adjustment screw somewhere on the probe or the near the BNC connector. Some probes adjust by twisting some part of the probe.
4) Find a small metal contact (usually near the scope screen) marked with a square wave (⎍⎍), "Probe Adjust", "Probe Comp", "Cal", "Calibration Output" or something similar. This is a square wave output provided by the scope specifically for probe adjustment. Connect the probe tip to this contact.
5) Adjust the scope controls to get a trace. You should see a good square wave if the probe is properly compensated.
6) If the leading edge of the square wave is distorted (rounded or peaked), adjust the probe for the best possible square wave (squarest). Bad⎍⎍ Bad ⎍⎍ Good ⎍⎍

PLL Circuit Problems I Have Seen

1. Bad wiring for the input from the Function Generator so that C_3 is shorted out.
2. Forget to connect pins 3 & 4.
3. If the power to the function generator is cycled, don't forget to reset it to 8 volts p-p square wave (shows 4 Vpp).