University of Utah
Electrical & Computer Engineering Department
ECE 3510 Lab 6
Basic Phase - Locked Loop

M. Bodson, A. Stolp, 2/26/06
rev,3/1/06

Note : Bring a proto board, parts, and lab card this week. You will build a circuit.

Objectives
- Learn the basic concepts of operation of phase-locked loops (PLL).
- Measure the gain of a voltage-controlled oscillator.
- Construct a PLL with a first-order filter.
- Measure PLL properties such as capture range, hold range, transient response, and steady-state ripple and correlate with analysis results.

Check out from stockroom:
- Wire kit
- Two 10x scope probes

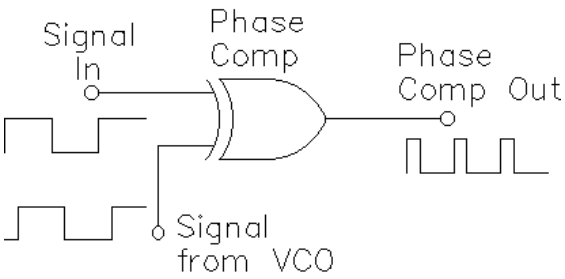
Parts to bring or buy:
- Proto board
- CD4046 CMOS PLL IC
- 1k, 10k, two 18k & a fifth resistor that will be determined in the lab
- 0.1µF, 0.01µF, 3900pF low temperature coefficient capacitor, & a forth capacitor that will be determined in the lab

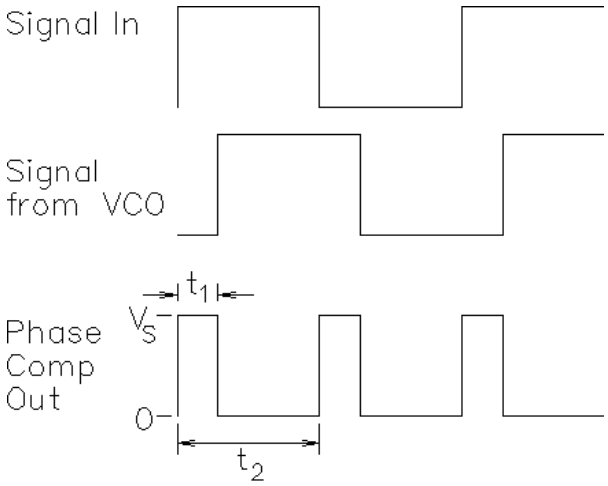
A WORD ABOUT STATIC

The PLL IC that you will be using is a CMOS part and is static sensitive. Following a few precautions will avoid zapping your IC.
- Ground yourself to your circuit before inserting the IC or working on the circuit. Never assemble or change your circuit with the power applied.
- Connect signal and power source ground leads first.
- Apply circuit power first, then signal sources. To change your circuit, remove signal sources first, then power.
- Disconnect signal and power ground leads last.

Introduction
A phase-locked loop (PLL) generates a signal whose phase is locked to the phase of an incoming signal. It consists of a voltage controlled oscillator (VCO), a phase detector and usually some type of low pass filter. The phase detector compares the output of the VCO to an incoming signal. The result of this comparison is a voltage applied to the VCO, usually through a filter. Phase-locked loops are used for the demodulation of frequency-modulated (FM) signals, for frequency synthesis (creating multiples of a reference frequency), and for other applications.

Pre-lab
This particular phase-locked loop IC contains two different phase detectors. The one we will use is simply an exclusive or (XOR) logic gate. See the drawing on the next page. It is a good phase detector for square-wave signals, assume they are. The output of the XOR phase detector switches between 0 and V_s. Assuming that the two input signals have the same frequency, sketch the output signal when the input signals are in phase (0° phase difference), then again when the input from the VCO lags the signal input by 90° (90° phase difference), and once more for 180° phase difference. Find the average (V_{avg} or





$$V_{avg} = \frac{t_1}{t_2} V_S$$

V_{DC}) for each of these outputs. What about negative phase differences? If you can't see what the average outputs would be for negative phase differences, then make sketches. Plot the average value of the output signal for a phase difference ranging from −180° to 180°. Notice that, within the range 0 →180°, the average value of the output of the phase is a linear function of the phase difference ($\theta - \theta_{vco}$) and can be written as

$$\phi = V_{avg} = k_{pd}(\theta - \theta_{vco})$$

Find the value of k_{pd} in V/rad when V_s = 12V. The voltage-controlled oscillator (VCO) of the PLL chip can produce a limited range of frequencies which depend on the external components. The VCO is biased so that the center frequency of this range is produced when the applied voltage is $V_s/2$. What phase difference produces this output of the phase detector? That's the phase difference that you should see when the PLL is locked at it's mid-range frequency.

Phase-locked loops and their applications are discussed in section 4.5 (p. 84) in the text. You may want to read this section.

Experiment

This lab covers two main tasks: measuring the "gain" (k_{vco}) of the VCO and designing a PLL with first-order filter. Sections of this lab and of the next lab use the same or very similar circuits. Therefore, don't disassemble a circuit before you look at the one to be built.

To insure repeatability in the experiments, the 3900pF capacitor in this lab should be a low temperature coefficient type. The small epoxy coated, shiny, smooth, brown capacitors with a 392G printed on them should work fine. Do not use the bigger, dull, brown rectangular or disc-shaped capacitors. (The 392 reads like a resistor code 39 x 10^2 pF.)

Measuring k_{vco}

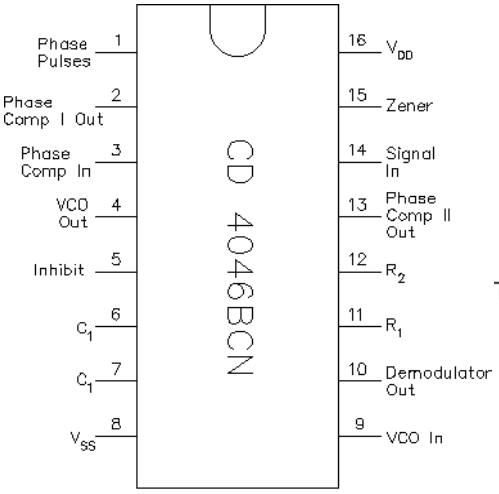
Begin by calibrating the 10x probes to your oscilloscope. If you are unsure of how to do this, check out the booklet titled "The XYZ's of Using An Oscilloscope," and read Chapter 8. The information is still useful even though the book is written for a different oscilloscope.

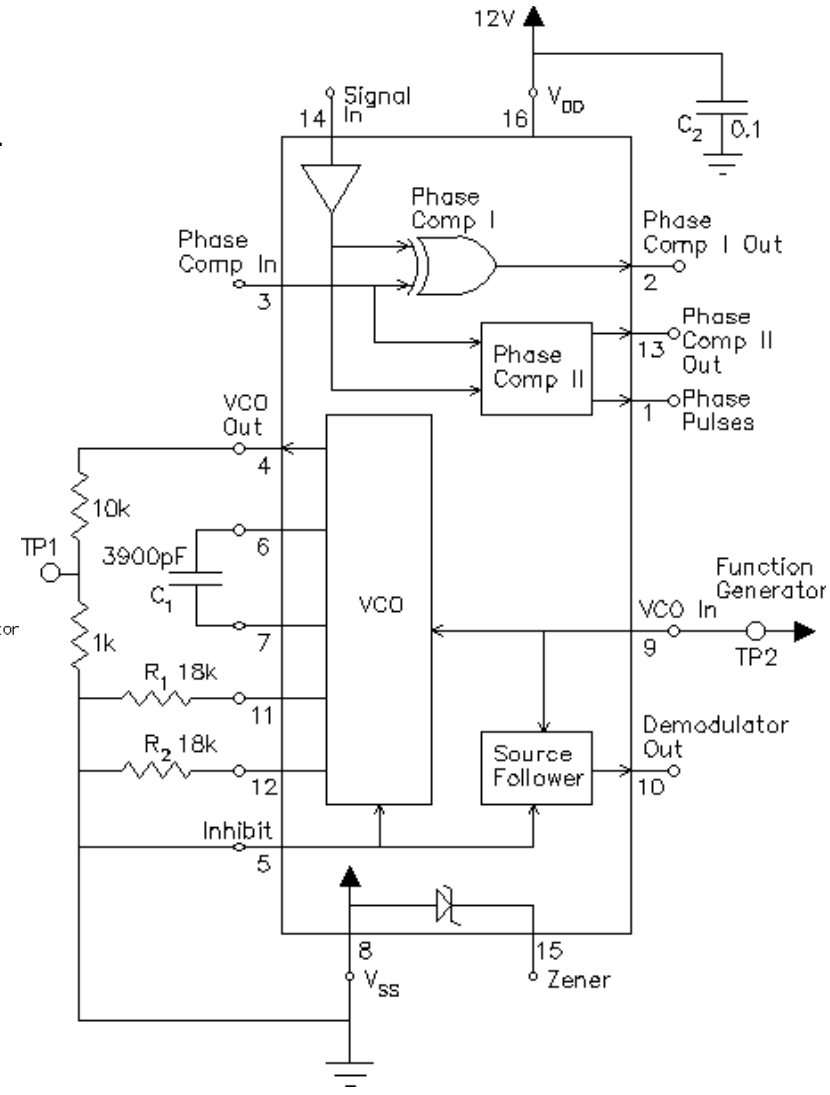
The purpose of a Voltage-Controlled Oscillator (VCO) is to produce a signal (square wave in this case) whose frequency is proportional to the input voltage.

$$f_{vco} = k_{vco} V_{vcoin}$$

The objective of this section of the lab is to find the constant of proportionality (k_{vco}).

Assemble the circuit shown at right on a proto board. Everything drawn inside the big box is inside the CD4046 PLL IC. The numbers around the box are the IC pin numbers.





Be sure to keep the 0.1μF capacitor (C_1) as close to the PLL IC as possible without trimming the leads. Notice that there are a number pins that we don't use. They are all output pins, so they can all be left disconnected.

The data sheet for the CD4046 indicates that with R_1 = 18kΩ , R_2 = 18kΩ, C_1 = 3900pF and V_S = 12V the VCO frequency range will be from 30kHz to 50kHz.

When you've built the circuit, connect the DMM to TP 2 (pin 9). Connect the power supply to V_{DD} (+) and Ground (-), turn it on, and adjust it to 12V. Turn on the function generator. Push and hold the DC offset until it displays DCV. Then it will output DC only (twice what the display shows). Connect it to TP2. Connect the scope to TP 1 to observe the output of the VCO and to measure the frequency of that output.

Adjust the VCO control voltage by adjusting the function generator DC offset voltage (+ voltages only). Make a table of frequencies for a number of voltages. Expect it to be

nonlinear below about 1V, so take a few readings there. It will also be nonlinear above 10V, in fact will nearly flatten out. To see this effect, temporarily lower the supply voltage to 10V and see what happens in the 8 to 10V VCO input range. Return V_S to 12V. Make a plot of frequency vs. voltage. Assume the plot is flat above 10V.

Determine the range of control voltage that results in a linear VCO frequency response. Determine the "gain" of the VCO, or k_{vco} (in Hz/V), in that linear range. Deduce the value of the Phase-Locked Loop gain ($k_{pll} = 2\pi k_{vco} k_{pd}$) using the value of k_{pd} determined in the pre-lab. Note that the transfer function from the VCO input to the output of the phase detector is then

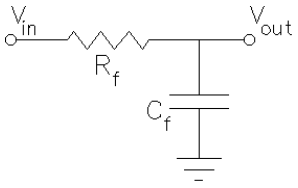
$$P(s) = \frac{k_{pll}}{s}$$

and constitutes the "plant" to be controlled.

Turn off the function generator and then turn off the output of the power supply.

Basic PLL

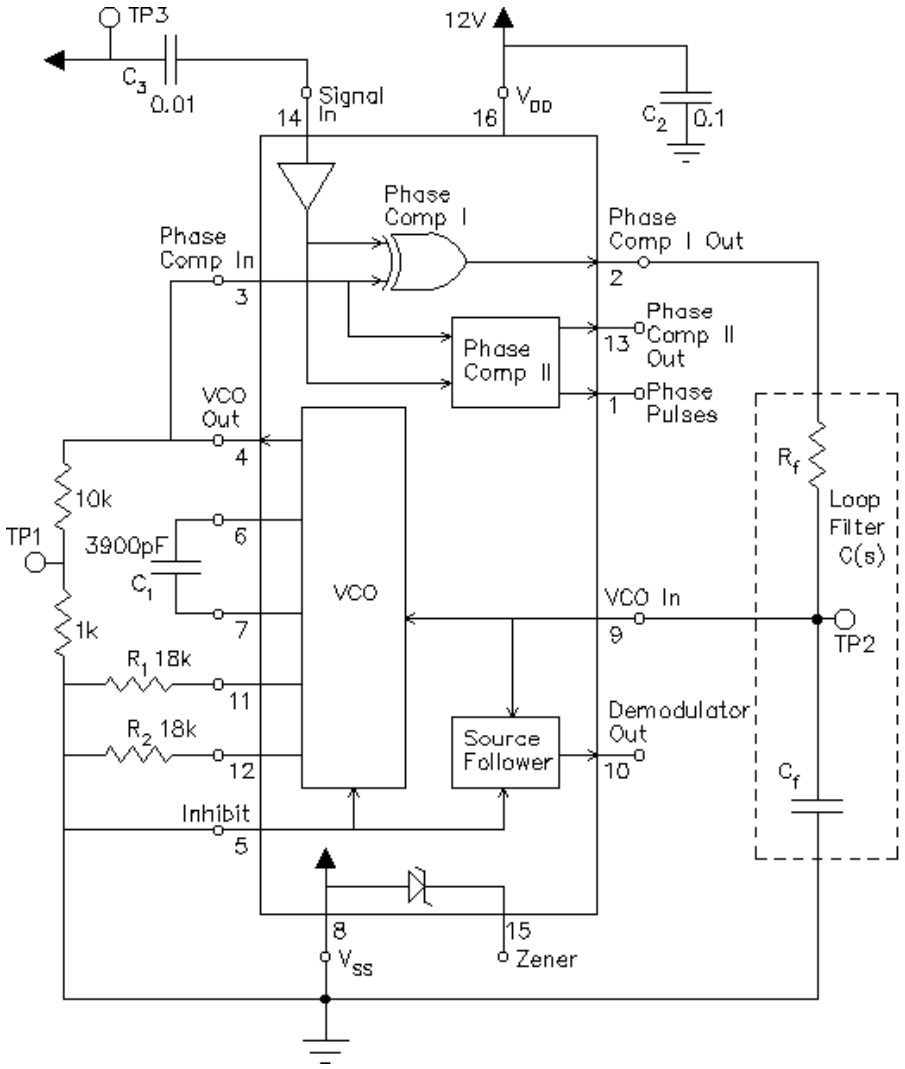
In this section, you will build a complete PLL circuit and measure its characteristics. It will include a first-order low-pass filter between the output of the phase detector and the input of the VCO. R_f and C_f together make make that simple RC filter.



Considering the circuit above, show that the transfer function of the loop filter (which takes the role of the compensator, C(s)) can be expressed in the form

$$C(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{k_f}{s + a_f}$$

Show that k_f and a_f both equal $1/R_fC_f$ (they turn out to be the same).



To get a desired damping factor of $\zeta = 0.707$ (see section 4.5.4 in the text), we need

$$a_f{}^2 = 2 k_{pll} k_f$$

Using the value of k_{pll} determined in the previous section, determine $R_f C_f$ (the product). Now you need to find values for the two components from this one equation, so you can arbitrarily select one of the two. From the list of standard values below (all in pF), select a C_f (possibly one you already have):

390, 470, 560, 680, 820, 1000, 1200, 1500, 1800, 2200, 3300, 3900, 4700pF

Given this value of C_f, determine R_f and see if it is close to a standard value between 10kΩ and 100kΩ. If not, try a different capacitor value. When you have values you like, construct the circuit above.

Test the circuit

Apply circuit power, turn on the function generator and set it to 40kHz, 8 volts p-p square wave, and connect it to the circuit through a coupling capacitor, C_3. With the scope, observe the signal input at TP 3 and the VCO output signal at TP 1. Trigger the scope on TP 3. With this set-up, the two waveforms on the scope should appear "in sync." In other words, the VCO waveform should be stationary and at the same frequency as the input waveform (the PLL is locked). If not, double check your PLL circuit and the loop filter values. Connect the DMM (set to DC) to TP 2 (pin 9), the VCO control voltage input. Print a copy of the scope screen for your notebook.

Slowly decrease the input frequency. Note that the VCO control voltage (shown on the DMM connected to TP 2) decreases as well. As you drop below 30kHz or so, you should notice that the VCO signal looses sync with the input signal. You can understand why if you remember how the VCO works from the first section of this lab and if you watch the DMM. In your lab notebook, explain why the PLL looses sync. See if the PLL will also loose sync if you adjust the input frequency too high. Between the limits you just found (~30kHz and ~50kHz), the VCO frequency should track the input frequency, does it do so? In the next paragraph you'll explore these limits in more detail.

Measure the PLL's hold range and capture range

The hold range is the range of input frequencies for which the PLL maintains phase lock. The capture range is the range for which the PLL acquires phase lock. To measure the lower edge of the hold range, start the input frequency at a point where the PLL is phase-locked, then reduce the input frequency until the PLL looses lock. The lowest frequency where lock can be maintained is the lower edge of the hold range. To measure the lower edge of the capture range, start the input frequency at a point where the PLL is not phase-locked, and raise the frequency until the PLL acquires phase lock. That frequency is the lower edge of the capture range. These two will be very close (if not the same). You will probably have to go in and out of lock a number of times at ever smaller frequency steps to find the lower edges to the nearest 10Hz. Find the upper edges the same way. Adjust the input frequency into the lock range.

Plot the phase difference vs. frequency
On the scope you should see two square waves, somewhat out-of-phase. In this section you'll vary the input frequency through the hold range and plot that phase difference vs. frequency. You only need to measure 4 or 5 frequency points, see the box for details of how to make the phase measurement. Does the phase remain constant over the input frequency range? Can you explain why not?

A QUICK REVIEW OF OSCILLOSCOPE PHASE MEASUREMENT

Measuring phase on the oscilloscope is quite easy. It is simply the measurement of the time between two points on two waveforms. The time measured is divided by the signal period and multiplied by 360 degrees to give the phase difference in degrees.

The Agilent scopes will perform this measurement for you if you push Quick Meas, Select Phase, Measure Phase and select the source you're not triggering on.

Observe the VCO input
Set the input frequency to 40kHz and measure the VCO control voltage input (TP 2 (pin 9)) with the scope. Is this control voltage a nice clean DC voltage? If not, how much ripple is present? What is the source of the ripple? Hint: use the other channel of the scope to observe pin 2 on the PLL and remember the time constant of the loop filter. Print a copy of the scope screen for your notebook.

In theory, the ripple could be decreased by lowering the bandwidth of the loop filter. However, the constants k_f and a_f cannot be set independently. To find out what would happen if the bandwidth of the RC filter was decreased, sketch the root-locus of the closed-loop poles as a function of a_f ($1/(R_f.C_f)$) The closed loop poles are the roots of

$$s^2 + a_f(s + k_{pll}) = 0$$

Notice that if the a_f factor were the gain (k) of a normal root-locus, then the open loop transfer function would be

$$G(s) = \frac{s + k_{pll}}{s^2}$$

Explain why increasing the time constant of the loop filter (decreasing a_f) is not desirable. Refer to p. 34 in the text and think in terms of a/b as the a_f term is decreased. If you want to, you can try to add a resistor in series with R_f and/or a capacitor in parallel with C_f to increase the time constant a little. See if the system still locks. If it does, set that extra resistor or capacitor aside for now and you can try it again later with the square-wave FM.

Frequency Modulate the input
Next, the input frequency will be modulated, first by a sine wave and then by a square wave to view the PLL step response. Set-up the function generator as shown below.

Buttons	Display		
Shift-FM (⊓)	1.000 kHz	adjust to:	**38.00 kHz**
Shift-Freq	10.00 Hz	adjust to:	**200.0 Hz** (Adjusts modulation frequency)

Shift-Level (Ampl)	DEVIATION		
Quicky changes to:	100.0 Hz	adjust to:	**5.000 kHz** (Adjusts modulation frequency change)

Observe TP 2 (pin 9) on the scope. Run a BNC to BNC cable from the SYNC output of the function generator to other channel of the scope and trigger on this channel. I also had to adjust the trigger level to get a stable trace. The fuzzy sine wave is the demodulated output signal. A cleaner version can be found on pin 10, but if you observe that, be sure to return the scope to TP 2 (pin 9) before you go on. Next you'll change the modulation to a square wave.

Set-up the function generator as shown below.

Buttons	Display	
Shift-Menu	A:MOD MENU	
v (down-arrow)	1:AM SHAPE	
>, > (Or turn knob)	3:FM SHAPE	
v	SINE	
> (Or turn knob)	**SQUARE**	(Adjusts modulation shape to a square wave)
Enter	ENTERED	

TP 2 (pin 9) should now have about a 5 volt p-p square(ish) wave. Describe the response of the VCO control voltage (TP 2 (pin 9)) in terms of speed of response, overshoot and noise (ripple). Print a copy of the scope screen for your notebook. If you found a longer time constant filter in the last section that works, try that again here. You may have to lower the deviation to make things work. Note the overshoot now. Print a copy of the scope screen again if you have something interesting.

Slowly increase the modulation (deviation) as shown below:

Buttons	Display	
Shift-Level (Ampl)	DEVIATION	
Quicky changes to:	5.000 kHz	slowly adjust up

If you adjust the deviation too high, the output frequency will shift beyond the hold range of the PLL and you'll see some interesting effects. Breath a sigh of relief, the lab is now over.

Conclusion Check - off and conclude as always. Do not take apart your PLL circuit. Most of it will be used next week in the advanced PLL lab.