University of Utah
Electrical & Computer Engineering Department
ECE 3510 Lab 7
Advanced Phase - Locked Loop

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Note : Bring circuit and lab handout from last week's lab.

Objectives
- Refine the design of the loop filter used in the basic PLL lab. You'll use a second-order filter in place of the first-order filter, and a better phase detector.
- The new filter is an example of control system design with integral action and lead compensation.
- Evaluate the improvements in performance
- Use your PLL to create frequency synthesizer

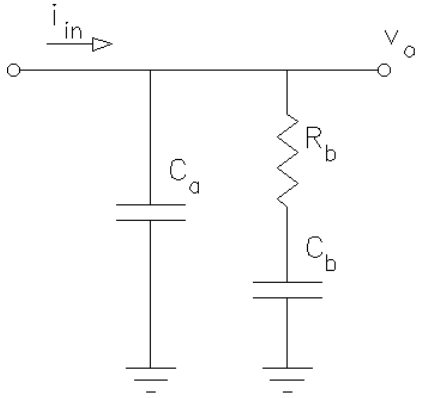
Check out from stockroom:
- Wire kit
- Two 10x scope probes

Parts to bring or buy:
- All parts from last week's Basic PLL lab, built around the CD4046 CMOS PLL IC
- 2- 470Ω, 2- 1k, 2- 500Ω trim pots (single turn), 4.7k, & 9.1k resistors
- 2- 0.01µF, 1200pF, 2- 0.01µF, & 0.015µF capacitors
- 2- 1N4148 diodes
- 2N3904 & 2N3906 transistors

Introduction
The basic PLL lab ended with testing a basic PLL with a first-order filter. While the experiments validated the design, the VCO input (FM demodulation output signal) contained a large amount of ripple. Often, such a high ripple is intolerable. In most communication systems, the ripple (or harmonic frequency content) of the loop filter output must be attenuated by 50 to 90dB. Unfortunately, the simple RC filter did not provide enough flexibility to improve the design. This lab demonstrates how a more sophisticated loop filter can reduce the output ripple while maintaining good tracking of the incoming signal.

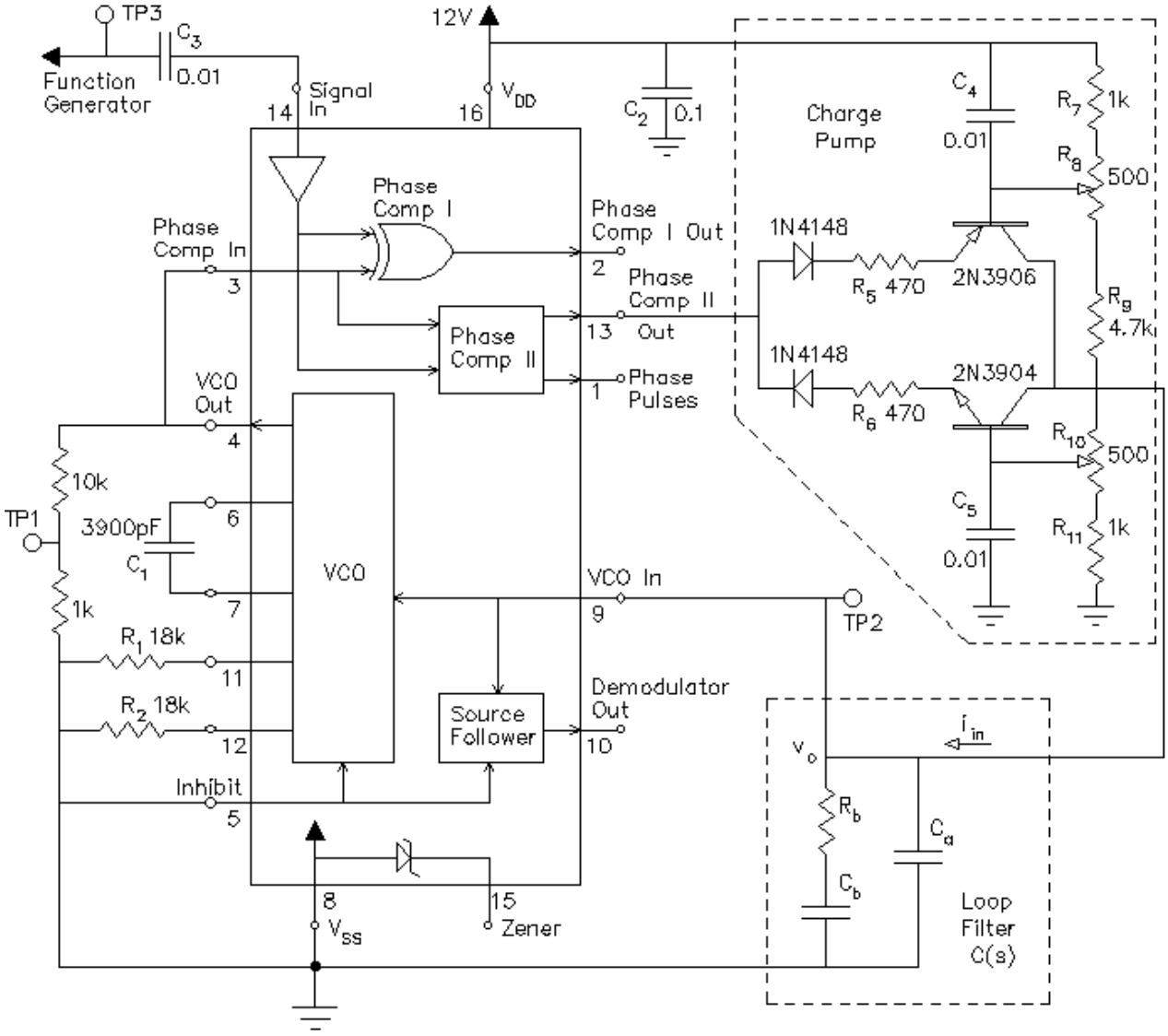
Pre-lab
Show that the filter shown at right has transfer function

$$C(s) = \frac{V_{out}(s)}{I_{in}(s)} = \frac{k_f(s+b_f)}{s(s+a_f)}$$



Find C(s) as a function of C_a, C_b, and R_b. Rearrange C(s) so that you can express k_f , a_f, and b_f in terms of C_a, C_b, and R_b.

Note that the input of the loop filter is a current, rather than a voltage. That means that the output of the phase detector must be converted from a voltage to a current. The voltage to current circuit that we will use is called a *charge pump*. The whole phase-locked-loop circuit is shown below, including the charge pump and the filter from the previous page as the loop filter.



Assume that the "plant" transfer function is $P(s) = \frac{kpll}{s}$ With $k_{pll} = 2.435 \frac{Amp}{Volt\,\sec}$

Write the full open-loop transfer function $G(s) = C(s)P(s)$

The three parameters of the loop filter (C(s)) are k_f, a_f, and b_f. In general, a_f needs to be greater than b_f (this type of control is called lead compensation). The locations of a_f and b_f on the real axis determine the location of the closed-loop poles. We will let

$$a_f = 86.96 \frac{krad}{\sec} \qquad \text{and} \qquad bf = 6.25 \frac{krad}{\sec} \qquad \left(\frac{krad}{\sec} = 1000 \frac{rad}{\sec} \right)$$

Plot the root-locus of the PLL system for varying gain ($k = k_{pll}k_f$) (use the Matlab function rlocus to check your results). Note that, for the values of a_f and b_f chosen, the root-locus has two break-away points. Compute:

1. The two break-away points
2. The gain ($k = k_{pll}k_f$) and closed-loop poles (s-values) associated with the break-away point that is reached first (right-most) as the gain increases. That will be our design goal. Deduce what the filter gain k_f should be.
3. Using Matlab, plot the step response of the closed-loop system from the scaled modulating signal x_s to the VCO input signal x_{vco}. Interpret the results.
4. Finally, from the values of k_f, a_f, and b_f, find the values of the filter parameters C_a, C_b, and R_b.

Experiment

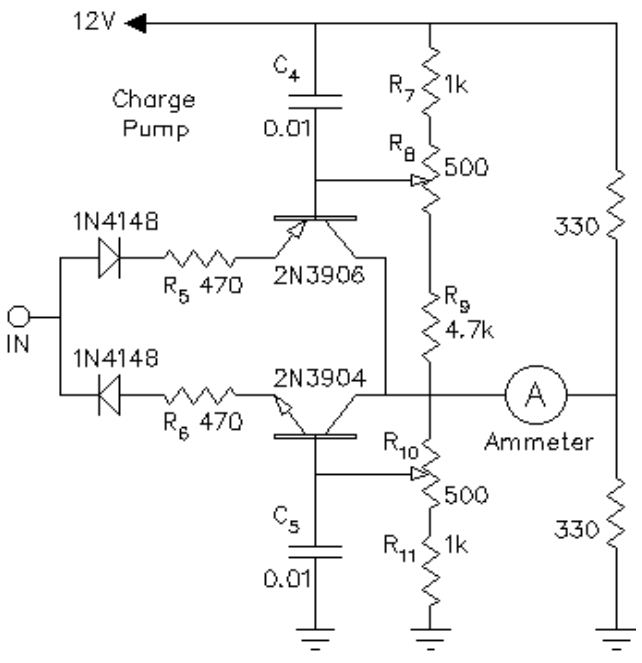
Introduction

The phase detector that was used in the basic PLL lab was a simple XOR gate. It detects differences in phase very well when the frequencies of it's inputs are the same, but it doesn't detect frequency differences very well. The loop filter had to be very carefully designed so that the PLL would still lock despite this phase detector's limitations. The downside was a filter with a short time-constant resulting in lots of ripple at the VCO input (which would be the demodulated signal if the PLL were used as an FM demodulator). That made it a lousy demodulator. But luckily the PLL IC includes a better phase detector as well.

Phase detector II (pin 13 output) is called a phase/frequency detector. It senses differences in frequency as well as phase. This property improves the ability of the PLL to acquire lock. Phase detector II also tends to lock the signals in phase, rather than in quadrature. Like the XOR gate, it produces voltage pulses whose width is proportional to the phase error. We're going to convert those voltage pulses to current using a charge pump conversion circuit. The purpose of the first part of this lab is to build and calibrate this circuit.

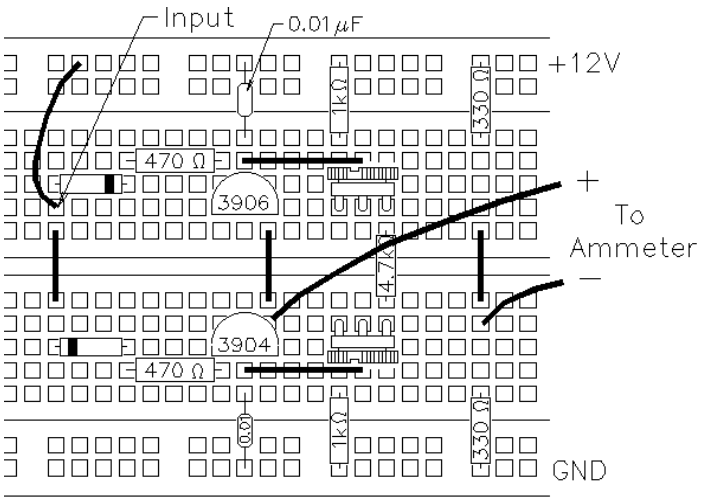
Construction and calibration of the charge pump

The circuit shown here is the charge pump form the schematic on the previous page with the ammeter and 330Ω resistors added for calibration purposes. Build it on your proto-board as shown on the next page. Leave a couple of inches of proto-board clear for future circuits. Hook the input to +12V instead of pin 13.



Notice how the layout on the next page matches the schematic part-for-part in position. Always try to try to draw your schematic as you can build it and make the layout match. It makes the circuit much easier to build and troubleshoot.

Double-check your circuit wiring, especially orientation of the transistors and the diodes. If you are confident that the circuit is wired correctly, apply power. If smoke came from your circuit, replace the bad parts and re-check. Next, calibrate the charge pump:



1. Adjust R_8, (the pot near the 2N3906) for an ammeter reading of roughly 600μA (0.6mA). If the ammeter reads 0.0 regardless of adjustment, check its connections (most meters have different connections for current measurements) and/or fuse. If the ammeter is working but you can't obtain the correct reading, check the top diode and the 2N3906 for proper installation.
2. Move the input connection from +12V to ground.
3. Adjust R_{10}, (the pot near the 2N3904) for an ammeter reading of roughly -600μA (-0.6mA). If you can't get that reading, check the bottom diode and the 2N3904 for proper installation.
4. That's only the rough calibration, next you'll calibrate to the phase detector output, which is not quite +12V and ground. Move the input connection from ground to pin 13 of the CD4046.
5. Hook the function generator to TP 3, turn it on and adjust it to show 4Vpp (it will actually output 8Vpp) at 60kHz (well beyond the hold range of this circuit). The phase detector output will now be at maximum.
6. Adjust R_8, (the pot near the 2N3906) for an ammeter reading of 600μA (0.6mA) +/- 2%. If you can't get that, you may have to change the value of R_7. A bigger value will mean more current.
7. Adjust the function generator to 20kHz (well below the hold range). The phase detector output will now be at minimum.
8. Adjust R_{10}, (the pot near the 2N3904) for an ammeter reading of -600μA (-0.6mA) +/- 2%. R_{11} can be changed if you can't get -600μA.
9. When calibration is complete, disconnect the ammeter and remove the two 330Ω resistors from your board.

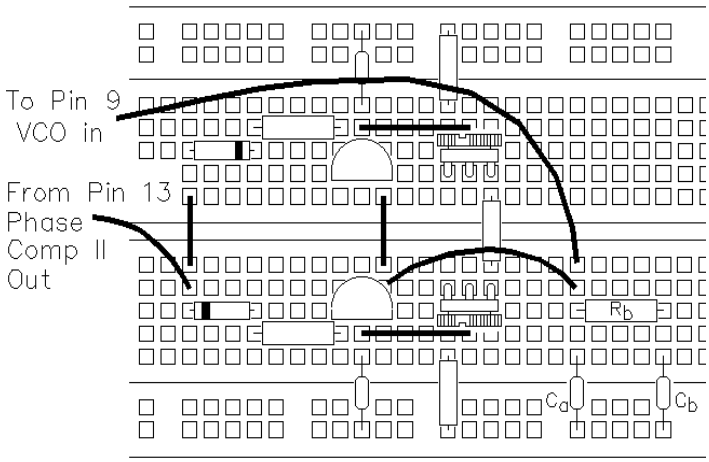
The maximum output of the phase detector will be +600μA for a +π phase shift and a minimum output of -600μA for a -π phase shift. Recall the value of k_{vco} from the last lab

and calculate the value of $k_{pd} = \frac{600\mu A}{\pi rad}$ and $k_{pll} = 2\pi k_{pd} k_{vco}$,

Do you get $k_{pll} = 2.435 \frac{Amp}{Volt\,\sec}$ as used in the pre-lab?

PLL with second-order filter

In the pre-lab, you found the values of C_a, C_b, and R_b for the loop filter. You bought parts that are close to these values. Add them to the circuit as shown. Remove the old loop filter and its connection to pin 9 before connecting the new filter.



Power-up the circuit and input a 40kHz 8Vpp sinusoid (shown as 4Vpp on function generator). Observe the signal input on TP 3 and the VCO output on TP 1 with the scope triggered from TP 3. Print a copy of the scope screen for your notebook.

Measure and record the PLL hold range and capture range as described in the basic PLL lab.

Vary the input frequency through the hold range and observe the phase difference vs. frequency. How does it compare to the plot you made in the last lab?

Measure the ripple of the VCO control voltage (TP 2). How does this compare with the measured ripple in the basic PLL lab? Print a copy of the scope screen for your notebook.

Find the section in the Basic PLL lab handout called "**Frequency Modulate the input**" Repeat that section for the new circuit. When you characterize the step response, find the time to settle within ± 10%? Compare the step response to that found earlier from theory.

Frequency Synthesis Using the Phase-Locked-Loop

In this section you're going to see what happens if you add a counter circuit between the VCO output at pin 4 and the phase detector input at pin 3. The output frequency from the counter is some integer division of the VCO frequency. The input frequency from the function generator will have to be lowered to match. That way you can create an output frequency (in the range of 30kHz to 50kHz) with a lower frequency input from the function generator. The higher frequency signal is said to be "synthesized" from the lower one. If the counter circuit is adjustable, then you may be able to synthesize a range of frequencies from a single input frequency. These synthesized frequencies will all be integer multiples of the input.

Ask your TA to demonstrate the circuit for you. Comment in your lab notebook.

Conclusion Check - off and conclude as always. You can now take apart your PLL circuit.