# Exam 3 Study Guide

# Fri, 4/15/22

The exam will be closed book, but you may use the colored sheets from exam 1 and 2 the new one for exam 3.

#### The exam will cover

- 1. Root Locus method
  - a) Main rules
  - b) Gain at any point on the root locus:  $k = \frac{1}{|\mathbf{G}(s)|}$
  - c) Additional rules.

The breakaway/in points are also solutions to:

Phase angle of G(s) at any point on the root locus:

$$\operatorname{arg}(G(s)) = \operatorname{arg}(N(s)) - \operatorname{arg}(D(s)) = \pm 180^{\circ}, \pm 540^{\circ}, \dots$$
  
Or: 
$$\operatorname{arg}\left(\frac{1}{G(s)}\right) = \operatorname{arg}(D(s)) - \operatorname{arg}(N(s)) = \pm 180^{\circ}, \pm 540^{\circ}, \dots$$

Departure angles from complex poles:



 $\sum_{all} \frac{1}{(s + p_i)} = \sum_{all} \frac{1}{(s + z_i)}$ 



## 2. Root - Locus Interpretation and design

Concepts of what a root locus plot is and what it tells you. Movement of poles

Good vs bad, fast response vs slow, OK damping vs bad.

Compensators

Know pole & zero locations of P, PI, lag, PD, lead & PID Compensators. PI and Lag, purpose and design, ties in with steady-state error PD and Lead, purpose and design ties in with root locus angle rules

**Choose points** on the s-plane to achieve given required characteristics based on the 2nd-order assumption (RL Crib) Know that the 2nd-order assumption may be inaccurate if other CL poles and/or zeros aren't 5x farther from Imaginary axis and are not canceling one another.

Design of a compensator to force the RL point through a given point (like RL7).

## 3. Unconventional root-locus

- 4. Compensator circuits & Instrumentation amplifier
- 5. PID tuning.
- 6. PLCs and Ladder logic. Basic switching logic.

7. **Bode Plots** (all types, including complex poles and zeros) Be able to draw both magnitude and phase plots and the smooth curves as well as the the asymptotic lines.

Bode to transfer function

GM, PM & DM

Bandwidth extension with feedback, Gain - Bandwidth product

- 8. Concentrate on Homeworks RL5 BP3
- 9. Up to Lab 7 (Advanced PLL)