UNIVERSITY OF UTAH
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
ECE 2280

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2/09

Lab #4 {200 pts} MOSFET TRANSISTORS

OBJECTIVES

- Understand the MoSFet operation.
- Find the process transconductance parameter along with the threshold voltage for both the p-type and n-type MosFet.
- To bias a NMOS transistor.
- To use a NMOS transistor in a common-source amplifier configuration and to measure its amplification.
- To study the effect of the source resistor and bypass capacitor on the amplification.
- To study the effect of a load resistor on the amplification.
- To build a common-source amplifier with active load (PMOS) and to measure the amplification. (BONUS assignment only).

Parts List:

☐ 1 kΩ, resistors
☐ 1 CD4007 chip
☐ 1 - 33 nF capacitor
☐ 1 - 0.1 microFarad capacitor
☐ 1 - 1 microFarad capacitor
☐ 1 - 10 kOhm resistor
☐ 1 - 50 kOhm resistor
☐ 2 - resistors: TBD
☐ 1 - 100 kOhm potentiometer

BACKGROUND INFORMATION:

***Precaution*: MOSFET transistors are very susceptible to breakdown due to electrostatic discharge. It is recommended that you always ground yourself before picking up the MOSFET chip. Do no touch any of the pins of the chip.**

MosFet Parameters and Operation:

Refer to example in Fig. 4.11 below. For this "enhancement-mode" n-MOSFET, the gate bias must be more positive than the threshold voltage V_t (e.g., +2 Volt), in order to induce a conductive channel and thus a measurable i_D. Further, the more positive the gate voltage is, the higher the drain current.

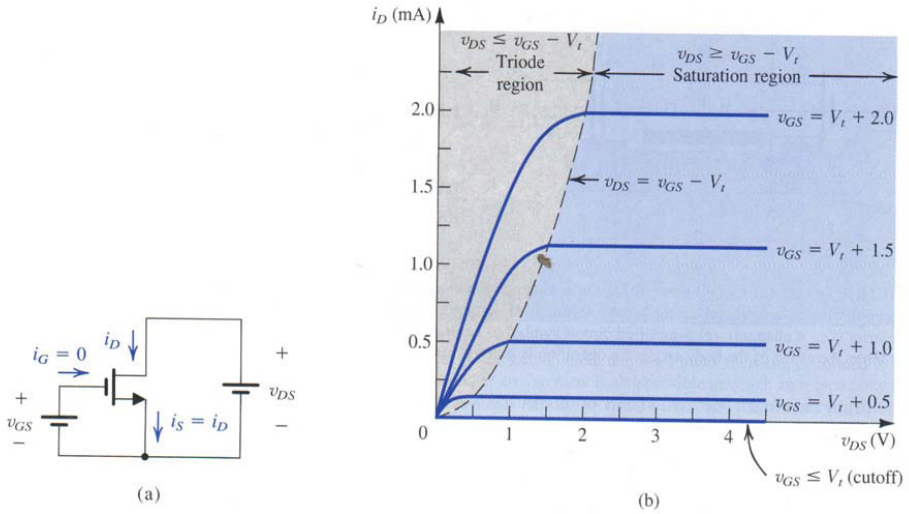


FIGURE 4.11 **(a)** An *n*-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)** The i_D–v_{DS} characteristics for a device with $k_n'(W/L) = 1.0$ mA/V^2.

In the text, section 4.2.2, there are equations that you need to follow. The end result is that there are these two operation regimes, and the corresponding equations describing i_D as a function of v_{DS} and v_{GS} are:

1. The "Triode region" is defined by $v_{DS} \le (v_{GS} - V_t)$, and

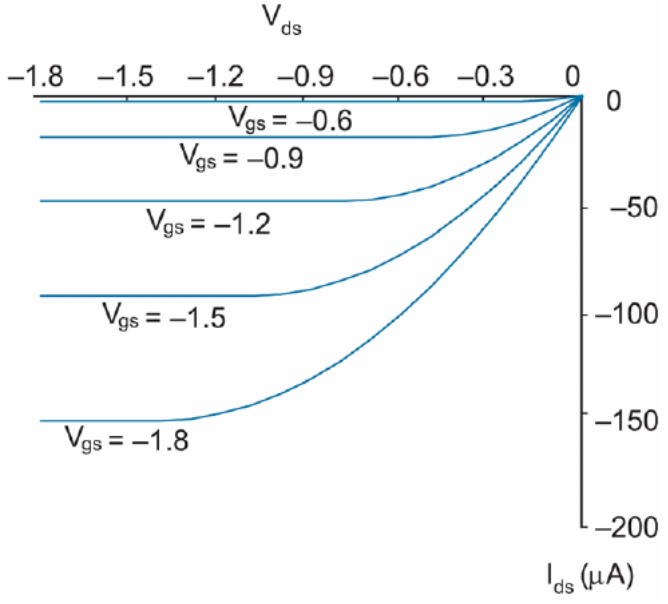
$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}(v_{DS})^2\right].$$

2. The "Saturation region" is defined by $v_{DS} \ge (v_{GS} - V_t)$, and

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 .$$

The two equations are derived by some assumptions related from the structure, doping profile, shape, material properties, transport mechanism, temperature, etc. By and large, they work well and can be used to predict the current within 10%.

The p-MOSFET is similar in structure, but now the conductive carriers are "holes," or, vacancy of electrons. Section 4.2.4 describes the characteristics of the p-channel MOSFET. An example is shown in the figure below. (From http://homepages.cae.wisc.edu/~kursun.)



Notice that the source is defined to be "the source of carriers." For p-MOS, in order to draw positive holes from the source to the drain, the drain-to-source bias should be negative. The gate-to-source bias should be more negative than the threshold voltage, for inducting holes at the channel. The threshold voltage for "enhancement-mode" pMOS is negative, for example, -2 Volt. There are also two operation regimes and the corresponding equations describing i_D as a function of v_{DS} and v_{GS} are:

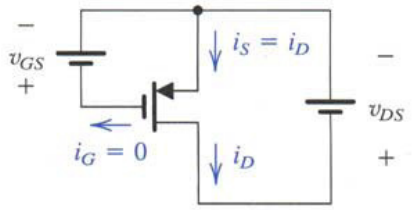
3. The "Triode region" is defined by $v_{DS} \geq (v_{GS} - V_t)$, and

$$i_D = k_p' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}(v_{DS})^2\right].$$

4. The "Saturation region" is defined by $v_{DS} \leq (v_{GS} - V_t)$, and

$$i_D = \frac{1}{2}k_p' \frac{W}{L}(v_{GS} - V_t)^2 .$$

Note that the sign of drain current i_D for pMOS is also positive. This is because of the convention defined in the textbook. See the circuit diagram taken from Fig. 4.18 below. The drain current for pMOS in this textbook is opposite to that defined for nMOS.



Biasing:

The common-source amplifier with a NMOS transistor is shown in Figure 1. The biasing is done by fixing the gate voltage with a voltage divider and also by using a source resistor R_S. The source resistor gives negative feedback and stabilizes the bias current as a function of temperature variations and transistor characteristics. This is a popular biasing scheme for discrete transistor circuits. Other biasing methods are possible, such as using a drain-to-gate feedback resistor, or using a constant-current source. The latter one is popular in integrated circuits. We will focus on the first method, illustrated in Figure B.1.

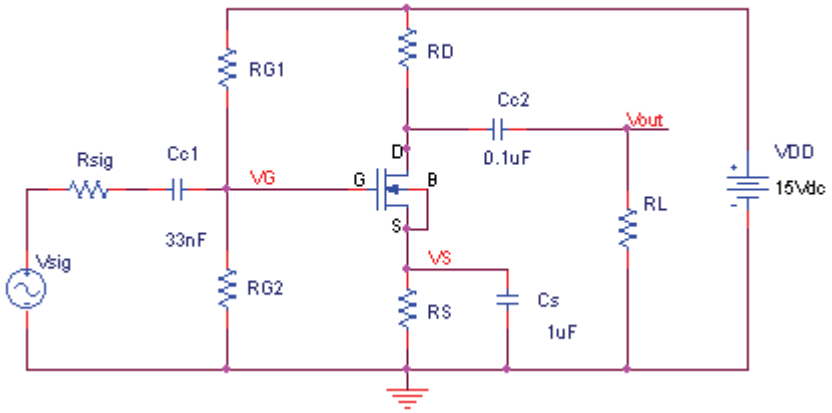


Figure B.1: Common-source amplifier in which biasing is done through a voltage divider and a source resistor. The input signal v_{sig} is coupled to the gate through a coupling capacitor C_{C1}. In this circuit we have connected the body terminal to the source terminal.

Biasing: Rule of Thumb

For proper biasing we can use the following rule-of-thumb. We select the source resistor value such that the voltage V_S at the source terminal is about one third to one fifth of the power supply V_{DD}. The resistance R_D is

chosen such that the drain voltage V_D is about in the middle of V_{DD} and V_S. This is done so that the signal at the drain has a relatively large and symmetrical output swing. These two conditions give us the resistor values of R_S and R_D for a specified drain current. The gate voltage can then be easily calculated as follows. Since the transistor is operating in the saturation region (see previous lab), we know that the current-voltage relationship is given by,

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2 \qquad \text{when } v_{DS} > (v_{GS} - V_t) \qquad (1)$$

Thus to obtain a certain bias current I_D we need to apply a gate-source voltage V_{GS} equal to,

$$V_{GS} = V_t + \sqrt{\frac{2I_D}{k_n' \frac{W}{L}}} \qquad (2)$$

The corresponding gate voltage V_G is than equal to,

$$V_G = V_S + V_{GS} = V_S + V_t + \sqrt{\frac{2I_D}{k_n' \frac{W}{L}}} \qquad (3)$$

Once the gate voltage V_G is known, one can find the values of the resistor R_{G1} and R_{G2}. We choose the resistors such that the parallel resistor is relatively large to ensure a large input resistance of the amplifier and prevent loading of the signal source $R_{in} = R_{G1} \| R_{G2}$.

The factor $(V_{GS} - V_t)$ is called the saturation voltage and corresponds to the minimal drain-source voltage required to keep the transistor in saturation. It is sometimes called the overdrive voltage.

$$V_{GS} - V_t = \sqrt{\frac{2I_D}{k_n' \frac{W}{L}}} = V_{DSat} \qquad (4)$$

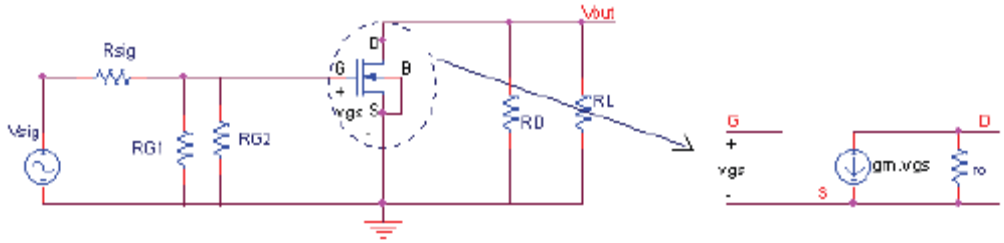
For the amplifier to operate properly one should make sure that the drain voltage does not go lower than

$$V_D > V_S + V_{Dsat} = V_G - V_t. \qquad (5)$$

This voltage will determine the output voltage swing.

Amplification

For signal frequencies of interest we can assume that the capacitors act as a short circuit what implies that the AC circuit can be drawn as shown in Figure B.2a. . The transistor can be replaced by its small signal equivalent circuit of Figure B.2b.



(a) (b)

Figure B.2 (a) AC circuit of the common-source amplifier and (b) the small signal equivalent transistor model.

$$g_m = \frac{\partial i_D}{\partial v_{GS}}|_Q = k_n' \frac{W}{L}(V_{GS} - V_t) = \sqrt{2 I_D k_n' \frac{W}{L}}$$

$$g_m = \frac{2 I_D}{V_{GS} - V_t} \qquad (6)$$

Thus the value of the transconductance depends on the bias current I_D.

The output resistor r_o is given by the ratio of the Early voltage ($=1/\lambda$) over the bias current,

$$r_o = V_A / I_D = 1/\lambda I_D. \qquad (7)$$

One can than easily calculate the expression of the amplification A_v,

$$A_v = -g_m (R_D \parallel R_L \parallel r_o) \approx -g_m (R_D \parallel R_L) \qquad (8)$$

The last approximation assumes that $r_o >> R_D \| R_L$.

The open-circuit voltage gain A_{vo} is the gain when R_L is removed $A_{vo} = -g_m R_D$.

In case the signal source has an internal resistance R_{sig} (not shown in Fig. 1 and 2), the value of the overall amplification will become,

$$G_v = -\frac{R_G}{R_G + R_{sig}} g_m (R_D \parallel R_L \parallel r_o) \approx -\frac{R_G}{R_G + R_{sig}} g_m (R_D \parallel R_L) \qquad (9)$$

Notice that the internal resistance forms a voltage divider with the resistance $R_G = R_{G1} \| R_{G2}$ which attenuates the input signal. It is for that reason that we need to keep the parallel resistance $R_{G1} \| R_{G2}$ large as compare to R_{sig} (see section on biasing).

The input resistance of the amplifier is equal to $R_G = R_{G1} \| R_{G2}$ and the output resistance $R_{out} = r_o \| R_D$. For a voltage amplifier one likes to keep the input resistance large and the output resistor small. For the common-source amplifier, the input resistance in large. However, the output resistance is also large. It is for this reason that by adding a load resistor R_L at the output, the output voltage and thus the amplification reduces. In order to obtain a small output resistance, one can add a common-drain (or source follower) configuration after the common-source amplifier.

Experiment 1: Finding MosFet Parameters (50 points)

It should be mentioned that the transistor characteristics of the CD4007 could vary considerably from chip to chip. The transistors may come from a different batch, what can explain why the threshold voltage, the transconductance parameter and the output resistance is different from the one used in the hand calculations and Spice simulation.

Procedure:

1. Connect the circuits in **Figures 1 and 2**.

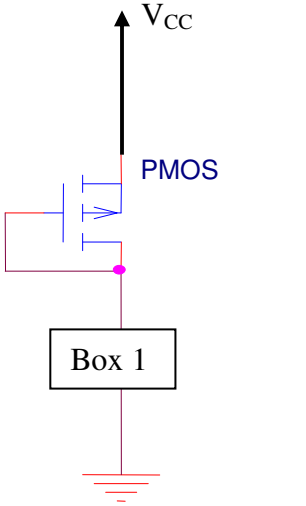


Figure 1. Measurement circuit to determine V_{tp} and K_p for p-type MosFets

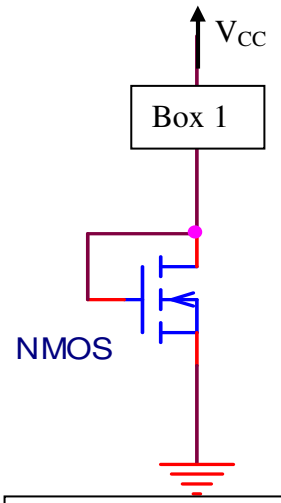


Figure 2. Measurement circuit to determine V_{tn} and K_n for n-type MosFets

2. Find the threshold voltage and K_p for the pmos. Select a pmos on the CD4007 chip or other discrete pmos device for this test.

(2a) (10pts) Apply voltage source of .5V for V_{CC} shown in Fig. 1. Place an ammeter in Box 1. Slowly increase the voltage at V_{CC} until you see current start to flow. This is the point where the transistor has transitioned from cutoff to being on. Estimate $V_{tp.}$

(2b) (15 pts) Add a 1k ohm resistor in series with the ammeter. Use V_{CC}=5V. Measure the new voltage between the drain and ground along with the current now flowing through the transistor. Use the saturation current equation to determine $K_p = k_p' \left(\frac{W}{L}\right)$.

3. Find the threshold voltage and K_n for the nmos. Select an nmos on the CD4007 chip or another discrete nmos device for this test.

(3a) (10 pts) Apply voltage source of .5V for V_{CC} shown in Fig. 1. Place an ammeter in Box 1. Slowly increase the voltage at V_{CC} until you see current start to flow. This is the point where the transistor has transitioned from cutoff to being on. Estimate $V_{tp.}$

(3b) (15 pts) Add a 1k ohm resistor in series with the ammeter. Use V_{CC}=5V. Measure the new voltage between the drain and ground along with the current now flowing through the transistor. Use the saturation current equation to determine $K_n = k_n'\left(\frac{W}{L}\right)$.

Experiment 2: Current Mirrors (50 points)

Procedure: Connect the circuit of **Fig. 3** (refer to pg. 286 - Fig. 4.33) Use 1 kΩ resistors for R_{REF} and R_L. The voltmeter across R_{REF} will allow you to calculate the current, I_{REF}, and the ammeter will allow you to measure the "output" current.

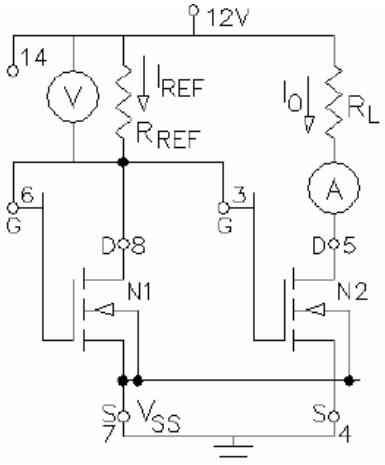


Figure 3. Current Mirror Configuration

1. (15 points) Turn on the power and determine I_{REF} and I_O, (They should be close to the same value.)

2. (15 pts) Record I_{REF} .

(2a) Measure and record the "output" current (I_O) for several loads, R_L = 1kΩ, 500 Ω (two 1k's in parallel), and 0 Ω (just the ammeter). Ideally, the load current will stay the same regardless of the value of the load resistor.

3. (10 points) Now try a different I_{REF}. Change R_{REF} to 500 Ω (two 1k's in parallel), find and record the new I_{REF}.

(3a) Measure and record I_O for R_L = 1kΩ, 500 Ω (two 1k's in parallel), and 0 Ω (just the ammeter) again.

4. (10 points) Current mirrors are commonly used in IC designs to provide bias currents. Explain in detail how they operate and how they can be used in an amplifier circuit.

Experiment 3: MosFet Amplifier (100 points)

{Refer to Section 4.5.2 and Section 4.7.3 from the Sedra-Smith, 5th ed. Book}

Work on 1-3 as a prelab if you do not finish the first week.

1. (10 pts) **Design the common-source amplifier** of Figure B.1 with a bias current I_D = 0.6mA. The source voltage V_S should be 3V and the drain voltage V_D should be chosen such that it is in the middle of V_S and $V_{DD.}$ The input resistance should be larger than 15 kOhm.

The NMOS transistor (CD4007 array) has the following characteristics:

V_t'=1.2V

k_n W/L=0.7mA/V^2

λ=0.004V^{-1}

γ=1.9 $V^{0.5}$ (note: since source-bulk terminal are shorted you won't need to use this value).

Use your measured values if using a discrete transistor instead of the CD4007 array.

a. Find the value of V_D.

b. Find the resistor values R_S, and R_D. Select values that are available in the lab.

c. Using the actual resistor value of R_S find V_S and V_G.

d. Find the values of the resistors R_{G1}, and R_{G2}.

e. What is the total DC power dissipation in the amplifier? (hint: power dissipation is $V_{DD} x I_{total}$).

2. (10 pts) **Analyze the AC circuit.** Using the values of the resistors and the bias current I_D, find the amplification of the amplifier:

a. Calculate the value of the transconductance g_m and small signal output resistor r_o.

b. Assume that no load resistance R_L is present, find the value of A_{vo}.

c. Calculate the voltage gain A_v for the case of a load resistance R_L=10 kOhm is added as shown in Figure B.1.

d. Assume that a source resistance R_{sig} of 5 kOhm is present, what is the effect on the overall amplification G_v? What is the value of the overall voltage gain G_v with both R_{sig} and R_L present?

e. What is the minimum voltage at the source in order to keep the transistor in saturation? What is the corresponding voltage swing?

f. Summarize the amplifier characteristics in table form: DC current and voltages (I_D, V_D, V_{Dmin}), total power dissipation, transconductance g_m, input resistance R_{in}, output resistance $Ro=R_D \| r_o$, amplification with and without load resistance R_L. Assume that signal source has a negligible internal resistance.

3. (15 pts) **Verify your design using PSpice**. You will need to use a model for the CD4007 transistor. The models can be downloaded from the class website. Save both the cd4007.lib and cd4007.olb files in your directory. The transistors are called nnmos for the NMOS and ppmos for the PMOS. You will need to add this library when drawing the schematic. Also, when creating a new Simulation Profile, while doing the simulation, you will need to add the library path and Filename (under the Libraries tab).
If you do not use the CD4007, you will need to locate a library and .olb file for your specific transistor. If you can not find a library for your part, simulate using the CD4007 libraries.

a. Enter the schematic of Figure B.1 without the load resistor R_L and coupling capacitor C_{C2}. Use your designed values. For the transistor you need to add the CD4007 Library or other library for your transistor.

b. Bias simulation. Simulate the circuit of Figure B.1 (without the load resistor R_L). Do a BIAS simulation and find the DC voltages at each node and current I_D. Compare the results with the one you calculated in #2 above.

c. Next, do a transient simulation. Use as input signal a sinusoidal source (Vsin) of 5 kHz frequency and amplitude of 0.2V. Do this first without a load resistor and next with a load R_L of 10 kOhm. Find the output voltage. What is the voltage amplification A_{vo} and A_v? Compare the simulation results with your hand calculations.

d. Do a frequency sweep (AC simulation) by replacing the input source by an AC source, Vac. Simulate the circuit with the load resistor of 10kOhm connected. Sweep the frequency from 10 Hz up to 100 kHz. Find the low-frequency cut-off point. Plot the Bode diagram of the amplification. Determine the low-frequency cut-off and mid-frequency amplification. How does the amplification compare with the one of the transient simulation?

e. Summarize the simulation results in table form in your notebook. Include all printouts in your notebook. Label each graph clearly.

4. Build and test the circuit.

You will be using the CD4007 MOSFET array in this lab. This array contains three NMOS and three PMOS transistors as shown in Figure 4. Again, the key point to remember is that the bulk (or substrates) of all NMOS transistors are connected to the VSS (pin 7) and all PMOS substrates are connected to VDD (pin 14). When using this array pin 7 should be connected to the most negative supply voltage or to the source of the transistor. Pin 14 is the substrate of the PMOS and must be connected to the most positive supply voltage in the circuit!

It should be mentioned that the transistor characteristics of the CD4007 could vary considerably from chip to chip. The transistors may come from a different batch, what can explain why the threshold voltage, the transconductance parameter and the output resistance is different from the one used in the hand calculations and Spice simulation.

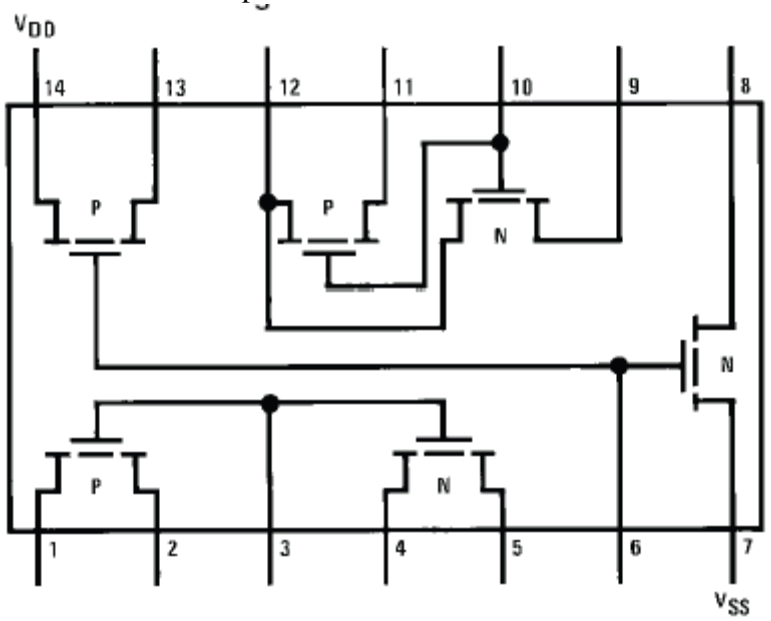


Figure 4: The CD4007 MOSFET array. *Pin 7* is connected to the substrate of the NMOS and *should be connected to the most negative voltage of the circuit (0r in some cases can be shorted to the source if and only if you use one NMOS transistor on the array!)*; pin 14 is the bulk of the PMOS and should be connected to the most positive voltage in the circuit.

Biasing of the transistor

The goal of this experiment is to bias the transistor of Figure B.1 according to the hand calculations. After building the circuit you will verify the biasing voltages and currents.

a. (5 pts) Build the circuit of Figure 5. Use the transistor between the pins 3, 4 and 5. Notice that we have connected the bulk (pin 7) to the source (pin 5) of the NMOS transistor. This can be done since we are only using a single NMOS transistor in the array. The reason for shorting drain-to-bulk is to eliminate the back-gate (body) effect on the threshold voltage. For the biasing resistor R_{G2}, use a100 kOhm potentiometer.

b. (10 pts) Measure the DC voltage at the drain. It is important is position the drain voltage V_D around 9 or 10 V. Adjust the potentiometer R_{G2} so that V_D is around 9V. After adjusting the gate voltage, measure the gate and source voltages. What is the corresponding drain current I_D?

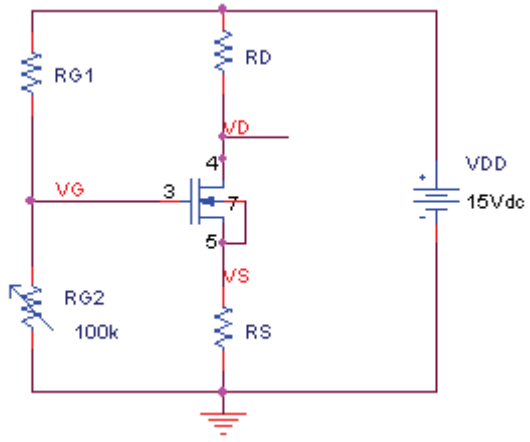


Figure 5: Biasing circuit of the common-source amplifier..

Common-Source Amplifier with Resistive load

Next you will use the transistor as an amplifier and measure its amplification and frequency response. You will also study the effect of the source and load resistors on the amplification.

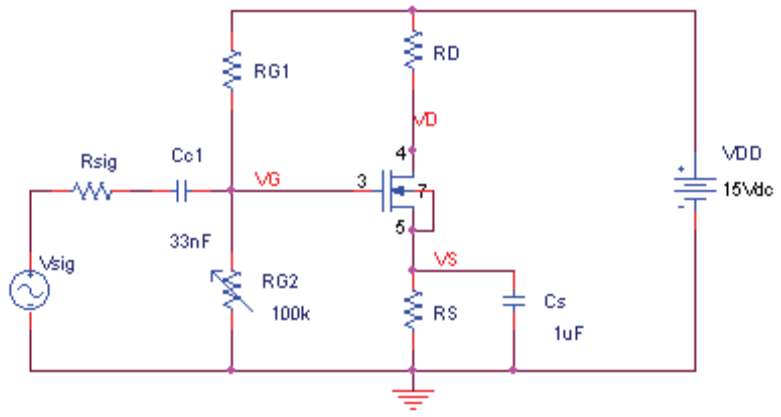


Figure 6: Common-source amplifier (Rsig is the internal resistor of the function generator and is about 50 Ohm).

c. (5 pts) Modify the circuit of Figure 5 by adding the capacitors C_{C1}, and C_S as shown in Figure 6. Connect a sinusoidal input signal of 0.2V amplitude (0.4Vpp) and 5kHz frequency.

d. (10 pts) Measure the voltage swing at the drain using the oscilloscope. Display the v_D on one channel and the input voltage v_{sig} on the other channel. Measure the peak to peak values of the input and output signal. What is the open-circuit amplification (voltage gain) A_{vo}? Notice the phase relationship. How does it compare to the calculated one? It should be mentioned that the transistor characteristics can vary considerably from chip to chip. It is not unusual the measured values differ by as much as 10-20% from the specified ones.

e. (10 pts) Increase the amplitude of the input signal and observe the output signal. When does the output signal start to distort? What is the maximum output voltage swing before considerable distortion occurs?

f. (5 pts) Lets remove the bypass capacitor C_S over the source resistor. Measure the output signal. What is the amplification? Notice the strong effect of removing the capacitor on the amplification.

g. (10 pts) Replace the capacitor C_S over the source resistor. Add the coupling capacitor C_{C2} and the load resistor R_L. as shown in Figure B.1. Use of C_{C2} a value of 0.1 uF and for R_L a value of 10 kOhm. Measure the output voltage v_O and the corresponding amplification A_v. Notice that the DC voltage has been removed from the output voltage. What happened to the amplification? Include a brief discussion on the effect of R_L.

h. (10 pts) Measure the frequency response of the amplifier with the load resistor connected. Change the frequency of the input signal. Starting from 5 kHz, reduce the frequency till the amplitude of the output has decreased by a factor of 0.707 (or 3dB). Record this 3dB frequency. What is the phase relationship between input and output signal? Next, increase the value of the input frequency till the amplification A_v reduces to 0.707 of its value at 5kHz. Record the high-frequency 3dB point. What is the bandwidth of the amplifier? What is the Gain-Bandwidth product? Explain the measured value of the low-frequency 3dB point? What causes this frequency cut-off?

BONUS Assignment Common-Source Amplifier with active PMOS Load (extra 20 pts)

This part is not required but can be done for extra credit (20 pts).

The goal of this experiment is to replace the drain resistor R_D by a PMOS transistor. We call this an active load. The advantage of doing so is: (1) larger resistor (i.e. the output resistance r_o) and thus a larger amplification; (2) no need to use a resistor. The latter is of particular importance for integrated circuits where large resistors are hard to make and occupy a large area.
The basic amplifier transistor is still the NMOS. However a current source has been replaced the load resistor R_D, as schematically shown in Figure 7a. The resistor R_G sets the gate voltage V_G and is kept very large in order not to load the input source. A current source can be implemented with a PMOS current mirror as shown in Figure 7b.

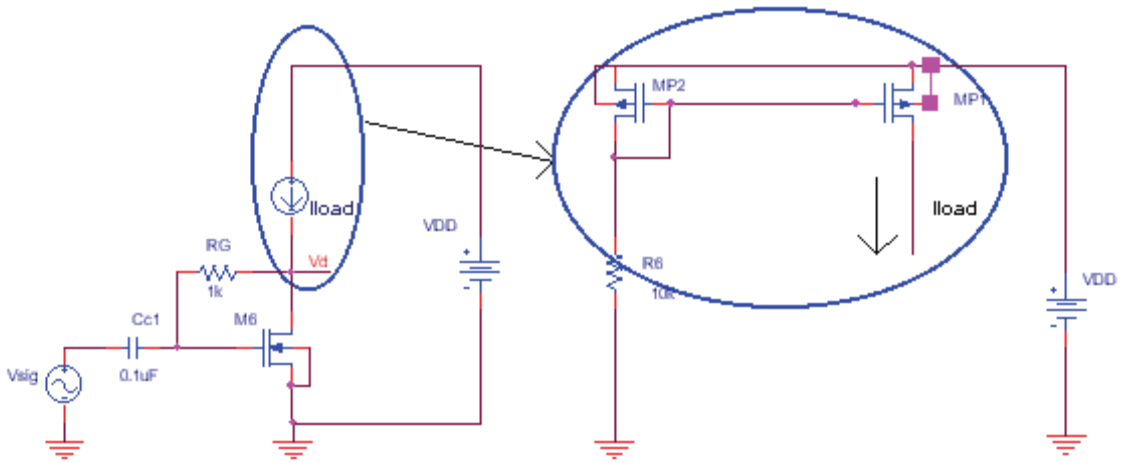


Figure 7 (a) Common-Source amplifier with a current source as the load; (b) the current source can be implemented by a PMOS current mirror.

By replacing the current source by the current mirror, we obtain the complete amplifier with active load as shown in Figure 8. We have also added a load resistor R_L and a coupling capacitor C_{C2}.

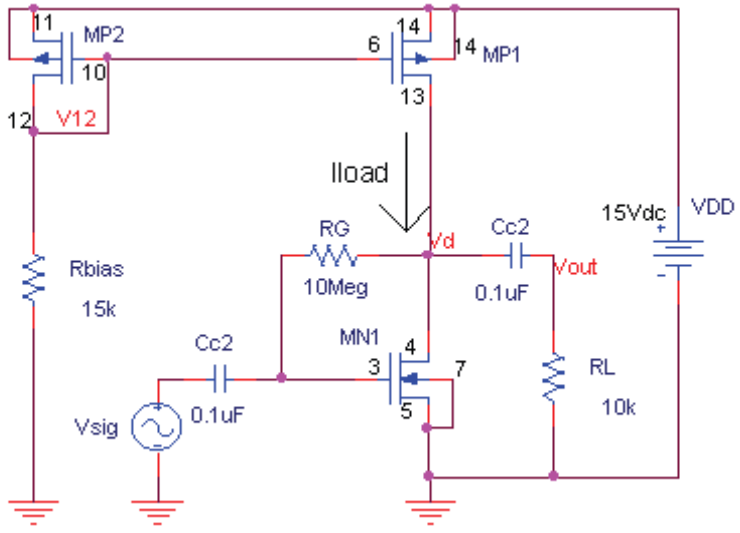


Figure 8: Common-Source amplifier with active load.

a. Build the circuit of Figure 8. For now do not include the load resistor R_L and a coupling capacitor C_{C2}. The pins of the transistor of the CD4007 array are given in the schematic. Use short jumpers on your protoboard to connect the pins of the transistors.

b. Measure the DC voltages V_{12}, and V_D. (and thus V_G) What is the corresponding drain current $I_D = I_{load}$?

c. Apply a sinusoidal input source Vsig with amplitude of 50mV and frequency 5kHz. Measure the output voltage v_d (do not include the load resistor or Cc2). If needed adjust the input amplitude to prevent distortion of the output signal. What is the open-circuit voltage amplification A_{vo}? What do you notice about the magnitude of the amplification, as compared to the one you measure on amplifier of Figure B.1?

d. Now connect C_{c2} and the load resistor R_L=10 kOhm. Measure the output voltage V_{out} over the resistor R_L. What is the amplification A_v? Notice the effect of the load on the amplification.

e. Discuss the effect of the active load on the amplification. Can you calculate the value of the amplification? (Hint: replace R_D in the expression of the amplification (8) by the parallel of the output resistances of the PMOS and NMOS transistors. Assume that the PMOS has the following characteristics: V_t=-1.0V, k_p' W/L=0.7 mA/V^2 and λ=0.035V^{-1}.