1. Referring to a forward biased pn junction diode, determine the following:
   a) For p-type and n-type material, state the majority and minority carriers (holes or electrons).
   b) Explain what happens as the temperature changes (increase and decreases) to the number of MAJORITY carriers in this p-type and n-type material?  
   c) Explain what happens as the temperature changes (increase and decreases) to the number of MINORITY carriers in this p-type and n-type material?  
   d) Explain in your own words, how the diffusion current, \( I_D \), is created.  
      when p-n junction is forward biased, depletion region becomes smaller and e- from n-type are injected into p-type which creates current flow \( I_D \).  
   e) Explain what happens as the temperature changes (increase and decreases) to the diffusion current, \( I_D \)?  

2. a) Draw the cross section of a mosfet.  

   b) Explain in your own words and drawings as needed how, when (under what conditions), and in what direction the current flows in the mosfet.  
   c) Explain in your own words all the different regions for Fig. 4.6 by drawing cross-sections of the mosfet to correspond to each region in that figure and explaining how each region operates (i.e. how the channel looks, how the current flows, etc.).

   d) Explain in your own words what the difference between Fig. 4.6 and Fig. 4.11.
   e) What equation and region of operation is graphed in Fig. 4.11.
   f) Explain in your own words how the PMOS differs from the NMOS transistor.

   \[ I_D \approx \frac{1}{2} k \cdot (V_{GS} - V_t)^2 \]

   Curve bends because the channel resistance increases with \( V_t \).
   Almost a straight line with slope proportional to \( V_t \).  

   \[ V_{DS} = (V_{GS} - V_t) \]

   Fig 4.6  

   Vos \approx (V_{GS} - V_t) \]

   Fig. 4.11
3. Analyze the circuit shown below to determine the voltages ($V_D$, $V_G$, $V_S$) at all nodes and the currents through all branches (5 currents). Let $V_t=1.5V$ and $k_n'(W/L)=2A/V^2$. Neglect the channel length modulation effect (i.e. $\lambda=0$).

\[ I_t = \frac{5}{50k} = 100 \mu A \]

\[ I_G = 0A \]

\[ V_G = 5 \left( \frac{25k}{50k} \right) = 2.5V \]

\[ I_D = I_S = \frac{1}{2} k_n'(W/L)(V_{GS}-V_t)^2 \]

\[ V_{GS} = V_G - V_S = 2.5 - 10(I_D) \]

\[ I_D = \frac{1}{2} (2)(2.5 - 10(I_D)) - 1.5 = (1 - 10I_D)^2 = 1 - 20I_D + 100I_D^2 \]

\[ 0 = 1 - 21I_D + 100I_D^2 \]

\[ I_D = \frac{21 \pm \sqrt{21^2 - 4(100)}}{200} = 0.137 \text{ or } 0.073 \]

\[ I_D = 0.137 \]

\[ V_{GS} = V_G - 1.37 = 1.13 < V_t \text{ (would be off)} \]

\[ I_D = 0.073A \]

\[ V_S = 0.73V \]

\[ V_D = 5V \]

**SATURATION conditions satisfied** $\Rightarrow$ $V_{BS} \geq V_{GS} - V_t$
4. Solve the circuits below to find $V_G$, $V_D$, and $V_S$. Find the currents in all branches. Assume $\lambda = 0$ and $k_n'(W/L) = 1\text{mA/V}^2$.

(a) Assume $sat$ =>

\[ I_G = 0 \]

\[ V_G = +4V \quad V_S = I_D(3k) \]

\[ I_D = \frac{1}{2}(1m)(4-I_D(3k)-1)^2 \]

\[ 2kI_D = (3^2 - 18kI_D + I_D^2(9k^2)) \]

\[ I_D^2(9k^2) - 20kI_D + 9 = 0 \]

\[ I_D = \frac{-20k \pm \sqrt{400m-324m}}{2(9k^2)} \]

\[ I_D = 20k \pm 8.7k \approx 1.6m, 628\mu \]

\[ I_D = 1.6m \Rightarrow V_S = 4.8V \]

\[ V_{GS} = 4 - 4.8 = -0.8V < V_T \times 90 \text{ off} \]

\[ I_D = 628\mu \Rightarrow V_S = 1.884 \text{, } V_{GS} = 2.110 > V_T \times \text{ on} \]

\[ +9 - I_D(3k) = V_D \]

\[ V_D = 7.116V \]

\[ V_{BS} \geq (V_{GS}-V_T) \times sat \]

(b) Assume $sat$ =>

\[ I = 0, V_G = +2V \]

\[ V_{GS} = +2V > V_T \times all \]

\[ I_D = \frac{1}{2} k_n'(\frac{W}{L})(V_{GS}-V_T)^2 \]

\[ I_D = \frac{1}{2}(1m)(+2-1)^2 \]

\[ I_D = 500\mu A \]

\[ V_D = +42 - 4kI_D \]

\[ V_S = +10V \]

\[ V_{BS} \geq (V_{GS}-V_T) \times sat \]

\[ V_S = 0V \]

(c) $V_{G2} = V_{D2} = +5V$

\[ V_{S1} = 0V \]

\[ I_D = \frac{1}{2} k_n'(\frac{W}{L})(+5 - V_{S1}-1)^2 \]

\[ I_D = \frac{1}{2} k_n'(\frac{W}{L})(V_{S2} - 1)^2 \]

\[ I_D = \frac{1}{4} k_n'(\frac{W}{L})(4 - V_{S2})^2 = \frac{1}{2} k_n'(\frac{W}{L})(V_{S2} - 1)^2 \]

\[ 4 + 1 = V_{S2} + V_{S2} \]

\[ V_{S2} = \frac{+5}{2} \]

\[ \Box \]

\[ I_D = \frac{1}{2}(1m)(5 - \frac{5}{2} - 1)^2 = 1.125mA \]

\[ I_D = \frac{1}{2}(1m)(\frac{5}{2} - 1)^2 = 1.125mA \]
5. Use: $V_i = 2V$, $K_n'(W/L) = 50 \mu A/V^2$, $\lambda = 0$

$V_I = 5 + 0.001 \sin(10t)$

Assume all capacitors are open for DC analysis and shorted for AC analysis

(a) Solve for the DC currents: $I_1$, $I_D$, and $I_S$
(b) Solve for the DC voltages: $V_G$, $V_S$, and $V_o$
(c) State the operating point, bias point, or quiescent point for this amplifier
(d) Draw the small-signal equivalent circuit
(e) Analyze the small-signal circuit for $V_o/V_I$.  

\[ I_1 = 0 \]
\[ I_D = I_S \]
\[ I_D = \frac{1}{2}(50\mu A)(V_{GS} - V_t)^2 \]
\[ V_{GS} = V_G - V_S \]
\[ V_G = 0 \]
\[ V_S = I_D(1k) - 10 \]
\[ I_D = \frac{1}{2}(50\mu A)(V_G - I_D(1k) + 10 - 2)^2 \]
\[ I_D = 50\mu A \pm \sqrt{\frac{1}{2}(50\mu A)^2 - 4(1k)^2(64)} = \] 1.2m, 54.8m

\[ V_S = -8.8V \]
\[ V_{GS} = 8.8V \text{ which gives } \Rightarrow I_D = 1.2m \]
\[ V_D = V_o = 15 - I_D(1k) = 13.8V \]
\[ V_{GS} = 22.6 \text{ } (V_{GS} - V_t) = 6.8V \]

\[ \text{bias point (operating point, or q point) is the voltage, } V_{GS}. \]

\[ V_g = V_I \frac{2 \mu m}{4 \mu m} = \frac{1}{2} V_I \]
\[ V_S = 0 \Rightarrow V_{GS} = \frac{1}{2} V_I \]
\[ V_o = -9mV_{GS} \frac{-1}{2} (1k) \text{ DC value} \]
\[ V_{GS} = K_n'(W/L)(V_{GS} - V_t) = 50 \mu A(8.8 - 2) \]
\[ V_{GS} = 340 \mu A/V \]

\[ V_o = 340 \mu A \frac{1}{2} V_I(50\mu) \]

\[ \frac{V_o}{V_I} = 85 \mu \text{m} \]
6. For the following hybrid-π equivalent circuit, find the following values:
(a) $R_i$ (input resistance – ignore the 10Ω and $V_{sig}$)
(b) $R_o$ (output resistance – ignore the 1k load)
(c) gain, $\frac{V_o}{V_{sig}}$
(d) Draw the transistor schematic of this circuit

\[ g_{m1} = \sqrt{(2(2m)1m} = 2m(2-1)^{\frac{1}{2}}m \]
\[ g_{m2} = \sqrt{(2(2m)4m} = 2m(3-1)^{\frac{1}{2}}m \]

a) \[ R_i = 1M \]

b) \[ R_o = 100 \Omega \parallel g_{m2} = 100 \parallel 250 \approx 71\Omega \]

c) \[ V_o = +g_{m2}V_{gs2} (100) \]

\[
\begin{align*}
V_{gs2} &= V_{g2} - V_o = -g_{m1}V_{gs1}(2k) - g_{m2}V_{gs2}(100) \\
V_{gs1} &= \frac{V_{sig}(1M)}{1M+10} \\
V_{gs2} &= -g_{m1}(2k)V_{sig} \\
&\quad \frac{1+g_{m2}(100)}{1+g_{m2}(100)} \\
\frac{V_o}{V_{sig}} &= \frac{g_{m2}(100)(-g_{m1})(2k)}{1+g_{m2}(100)} = -1.14V/V
\end{align*}
\]

d) \[ V_{gs1} = 2V \]

\[
\begin{align*}
V_{gs2} &= 4m(100) = 0.4V \\
V_{g2} &= V_{gs2} + V_{s2} = 3 + 0.4 = 3.4V \\
(3.4V = V_{g2}) &= V_{DD1} - 1m(2k) \\
&\quad V_{DD1} = 5.4V \\
V_{DD2} - 4m(1k) \geq (V_{g2} - V_t) = 3.4 - 1 = 2.4V
\end{align*}
\]

\[ \therefore V_{DD2} \geq 2.4 + 4 = 6.4V \]
7. For the circuit shown below, draw the AC small-signal equivalent circuit (use hybrid-π or model T). Make sure that everything is labeled in terms of the transistor number. (e.g. $g_m1$, $v_{gs2}$, etc.). $\lambda=0$ for all transistors. $v_{sig} = 0.001 \sin(10t)$ AC and $V2=10V$ DC.

8. $v_{sig} = (8+0.01\sin(\omega t))$ Volts. Does this circuit operate as a linear AC amplifier? If so, what is the gain, $\frac{V_o}{V_{sig}}$, of the following circuit in terms of $VDD$, $Vsig$, $Rsig$, $k'(W/L)$? If not, explain why. The graph below shows measurements for this circuit.

This mosfet is biased at a gate voltage of $V_G=8V$ and $V_S=0$.

$\therefore V_{GS} = 8V$.

It looks like the transistor will be in triode $\Rightarrow$

$V_{DS} > 0 \Rightarrow (V_{GS} - V_C) = 8 - 1 = 7V$

$\therefore$ TRIODE Region $\Rightarrow$ will not amplify linearly