Class Load
Syllabus & tentative schedule outline the workload for this semester. This is a very busy class. Every week will require **AT LEAST 10 HOURS** of outside studying to pass class.

ECE3700 + ECE2280 = Very busy semester – **Organize your time!**

**How can you survive??**
1. Easiest way to get through school is to actually learn and try to retain what you are asked to learn.
   - Even if you're too busy, don't lose your good study practices. What you "just get by" on today will cost you later.
   - Don't fall for the "I'll never need to know this" trap. Sure, much of what you learn you may not use, but some you will need, either in the current class, or future classes, or maybe sometime in your career. Don't waste time second-guessing the curriculum, It'll still be easier to just do your best to learn and retain.

2. Don't fall for the "traps".

3. KEEP UP! Use calendar.

4. Make "**PERMANENT NOTES**" after you've finished a subject and feel that you know it.

**REVIEW:**
- KVL, KCL, OHM'S LAW, THEVENIN EQUIVALENCE, OPAMPS
  a. Derive an expression for $I_1$. The expression must not contain more than the circuit parameters $\alpha, V_a, R_1,$ and $R_2$ (**Make sure to eliminate $V_2$ from the answer**). $\left(\alpha \neq 1\right)$

\[
\begin{align*}
V_{\text{loop}}: & \quad + \alpha V_2 - V_a - V_2 = 0 \\
V_2 (\alpha - 1) & = V_a \\
V_2 & = \frac{V_a}{(\alpha - 1)}
\end{align*}
\]

\[
\begin{align*}
\text{voltage loop} & \quad - I_1 R_1 + V_2 + V_a = 0 \\
I_1 & = \frac{V_2 + V_a}{R_1} - \frac{V_a}{(\alpha - 1) R_1} + \frac{V_a (\alpha - 1)}{R_1 (\alpha - 1)} \\
I_1 & = \frac{V_a + V_a \alpha - V_a}{(\alpha - 1) R_1} = \frac{V_a \alpha}{(\alpha - 1) R_1}
\end{align*}
\]
Thevenin Equivalence:

**CASE 1:** Thevenin Equivalent (circuit with only independent sources)

Step 1. Turn off all independent sources. (This means \( V = 0 \) (short) and \( I = 0 \) (open))

Step 2. \( R_{th} = \) equivalent \( R \) seen between the two desired nodes a-b.

Step 3. \( V_{th} = \) open circuit voltage between a-b.
**ECE2280 Fundamentals of Electrical Engineering**

**Case 2:** Thevenin Equivalent (circuit with dependent sources)

Step 1. Calculate the open circuit voltage, \( V_{th} \).

Step 2. Calculate \( R_{th} \). Use only one of the methods below:

Method 1: **TEST SOURCE**

(a) Remove all independent sources.

(b) Apply a voltage source \( V_{test} \) between \( a-b \) and determine the resulting current \( I_{test} \). (OR apply a current source \( I_{test} \) between \( a-b \) and determine the resulting voltage \( V_{test} \). Using 1V or 1A as the value of the applied test sources allow easy multiplication or division)

(c) \( R_{th} = V_{test}/I_{test} \)

Method 2: **SHORT CIRCUIT**

(a) Short circuit between \( a-b \) and find \( I_{sc} \), short circuit current.

(b) \( R_{th} = V_{th}/I_{sc} \)

**Example, Case 1:** (independent sources) Find Thevenin across \( R_2 \) (Removing \( R_2 \) from the circuit).


**Example Case 2:**

Find Thevenin between \( a-b \).

Step 1: (Find \( V_{open \ circuit \ voltage} \))

\[
V_{th} = \frac{-40i_2}{3} \cdot 10v_1 = V_g
\]

\( V_{th} \)

Dr. Rasmussen  
Spring 2011
(a) Remove all independent sources.
(b) Apply a test source (I_{test} in this case). Analyze circuit for V_{test} = V_o in this case.

\[ V_o = V_{test} = (10\|40) \times (I_{test} - 5i_2) \]

\[ i_1 = 0 \]
\[ v_1 = 3v_1(3) \Rightarrow v_1 + 9v_1 = 0 \Rightarrow v_1(10) = 0 \Rightarrow v_1 = 0 \]
\[ i_2 = 0 \]
\[ V_{test} = 8I_{test} \]
\[ R_{th} = 8I_{test}/I_{test} = 8 \text{ ohm} \]

**Step 2:**
**Method 2: SHORT CIRCUIT**

\[ i_{sc} = -5i_2 \]
\[ V_{th} = -5i_2(10\|40) = -40i_2 \]
\[ R_{th} = V_{th}/i_{sc} = -40i_2/-5i_2 = 8 \text{ ohm} \]

**SAME**

Note: Use of the Isc is sometimes easier than the test source. Suggest trying that method first. Both methods can be used to “check” the other one.

**DC Review Notes**

- **KCL (Kirchhoff’s current law):** \( \sum I_{in} - \sum I_{out} = 0 \) at any point.
- **KVL (Kirchhoff’s voltage law):** \( \sum V_{in} - \sum V_{out} = 0 \) around any loop.
- **Ohm’s law (resistive):** \( V = IR \)
- **Power:** \( P = \frac{V^2}{R} \) for resistive circuits
- **Series:** \( R_{eq} = R_1 + R_2 + \ldots \)
- **Parallel:** \( \frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + \ldots \)
- **Voltage divider:** \( V_o = \frac{R_o}{R_1 + \ldots + R_n} \)
- **Current divider:** \( I_o = \frac{R_o}{R_1 + \ldots + R_n} I_1 \)

**Suggested method:**
1. **First:** Check one method (series or parallel) to get a preliminary result.
2. **Second:** Use the other method to check the preliminary result.
3. **Third:** Use both methods to cross-check the results.

**Linear elements:**
- Assume a linear region and try the value.
Example #3

Solve for $I$, $I_1$, $I_2$, and $V_1$:

\[ I = \frac{12V}{2k+3k} = \frac{12}{2k + \left(\frac{3k(6k)}{3k+6k}\right)} = \frac{12}{2k + 2k} = 3mA \]

\[ I_1 = \frac{V_1}{3k}, \quad I_2 = \frac{V_1}{6k} \]

\[ I = I_1 + I_2 = V_1 \left(\frac{1}{3k} + \frac{1}{6k}\right) = V_1 \left(\frac{6k}{6k}\right) = \frac{1}{2k} \Rightarrow V_1 = I \cdot 2k = 3m(2k) = 6V \]

\[ I_1 = \frac{6}{3k} = 2mA; \quad I_2 = \frac{6}{6k} = 1mA \]

Example #4

Given $V_g = 6.25mV$, find $V_o$. Find the Thevenin equivalent between terminals a-b.

\[ V_{th} = V_o \quad \Rightarrow \quad \text{Therefore find} \quad V_o : \]

\[ V_o = \left(\frac{50 \Omega}{12.5 \Omega}\right) \cdot \left(-50i_2\right) = -500i_2 \quad \text{unknown} \]

\[ \frac{50}{12.5 + 50} = 10 \Omega \]

\[ \Rightarrow \quad i_2 = \frac{V_i}{100} = -20i_1 \cdot \left(\frac{25}{100}\right) = -20i_1 \cdot \frac{25}{100+25} = -4i_1 \quad \text{unknown} \]

\[ \Rightarrow \quad i_1 = \frac{V_3}{10 + 40} = \frac{6.25m}{50} = \frac{125m}{50} \quad \text{No unknowns} \]

\[ \Rightarrow \quad i_2 = -4i_1 = -4(1.25m) = -5m \]

\[ V_{th} = V_o = -500i_2 = +500(1.5) = 750V. \]
$R_{th} = \frac{V_{th}}{Isc}$, where $Isc$ is the short circuited current =>

From the analysis for $Vth$ (above). $Vth=-500i2$
$Isc=-50i2$ so

$Rth=-500i2/-50i2=10\text{ohm}$

(note that for this circuit configuration, it appears that the output $R$ ($Rth$) that the "top" of the dependent current source looks like an "open" so that the equivalent $R$ is $50||12.5=10\text{ohm}$).
Signals
A DC (direct current) signal refers to a fixed voltage whose polarity never reverses. {Ex. 5V, -15V}

An AC (alternating current) occurs when charge carriers periodically reverse their direction of movement. {Ex. Sinusoid => 5sin(10t), Square Waves, Sawtooth-shaped}
  • The voltage of an AC power source changes from instant to instant in time.
  • Wall plug is AC with a frequency of 60 hertz and 120V
    o 120*(1.414) peak value
  • RMS value = peak value/$\sqrt{2}$

Real signals such as your voice, environmental sensors, etc. are time-varying voltages or currents that carry information.
  • Transducers transform one form of energy into another:
    o Ex: Microphone, Camera, Thermistor or other thermal sensor, Potentiometer, Light sensor, Computer, etc.
  • Sine waves are "pretend" signals
    o Although sine waves are not real signals, we use them to simulate signals all the time, both in calculations and in the lab. This makes sense because all signals can be thought of as being made up of a spectrum of sine waves.

These types of signals can be hard to characterize mathematically. If a signal is periodic but arbitrary in amplitude, recall that it can be expressed by the Fourier series (a series of sinewaves of different frequencies and amplitudes).

Example #5
Sketch the following waveforms. Identify the dc component of the waveform and the ac component of the waveform.

a. $V_s=5\sin(10t) \ V$

b. $V_s=2V +4\sin(5t+90^\circ) \ V$

c. $V_s= 1V \pm 1V$
Sine wave:
Time domain:

![Sine wave graph](image)

Frequency domain:

Example #6
When analyzing a time dependent element (capacitors), translate into frequency domain \( C = \frac{1}{j\omega C} = \frac{1}{sC} \) and then analyze the circuit using normal circuit analysis techniques. Analyze the circuit to the right to find the transfer function \( \frac{V_o}{V_i} \). Solve the circuit symbolically first (with \( R_1, R_2, R_3, C \)) and then plug in their values.

![Circuit diagram](image)

\[
\begin{align*}
V_i &= \frac{R_3 \cdot V_i}{R_3 + R_1}, \\
R_{th} &= R_1 \parallel R_3
\end{align*}
\]

\[
\begin{align*}
V_o &= \frac{R_2}{(R_1 + R_3)([R_2 + R_1]\parallel R_3)(\omega^2)} \cdot V_i \\
&= \frac{20(10n)}{(10 + 20)(200.7n) \cdot (10n)S + 1)} \\
&= \frac{(133n) \cdot S}{(200.7nS + 15)} \\
\frac{V_o}{V_i} &= \frac{4 \times 10^{-5} \cdot S}{30(200.7nS + 1)}
\end{align*}
\]

What does this equation mean? By substituting \( s = j\omega \) in the above equation. The magnitude of the equation is:

\[
\left| \frac{133n(\omega)j}{(266.7n(\omega)j + 1)} \right| = \left| \frac{133n(\omega)j}{(266.7n(\omega)j + 1)} \right| = \frac{133n(\omega)}{\sqrt{(266.7n(\omega))^2 + 1^2}}
\]
This magnitude can now be graphed with the x-axis as $\omega$ and the y-axis as the calculated value. This is one of the graphs used for the Bode plots. To plot this, an understanding of dB is needed.

**Decibels**

Your ears respond to sound logarithmically, both in frequency and intensity. Musical octaves are in ratios of two. "A" in the middle octave is 220 Hz, in the next, 440 Hz, then 880 Hz, etc... It takes about ten times as much power for you to sense one sound as twice as loud as another.

A bel is such a 10x ratio of power. Power ratio expressed in bels = $10 \log \left( \frac{P_2}{P_1} \right)$ bels. The bel is named for Alexander Graham Bell.

It is a logarithmic expression of a unitless ratio (like gain).

The bel unit is never actually used, instead we use the decibel (dB, 1/10th of a bel).

Power ratio expressed in dB = $10 \log \left( \frac{P_2}{P_1} \right)$ dB

dB are also used to express voltage and current ratios, which related to power when squared. $P = \frac{V^2}{R} = I^2R$

Voltage ratio expressed in dB = $10 \log \left( \frac{V_2}{V_1} \right)$ dB

Current ratio expressed in dB = $20 \log \left( \frac{I_2}{I_1} \right)$ dB

These are the most common formulas used for dB

Some common ratios expressed as dB

- $20 \log \left( \frac{1}{\sqrt{2}} \right) = -3.01$ dB
- $20 \log \left( \frac{1}{2} \right) = -6.02$ dB
- $20 \log \left( \frac{1}{10} \right) = -20$ dB
- $20 \log \left( \frac{1}{100} \right) = -40$ dB

We will use dB fairly commonly in this class, especially when talking about frequency response curves.

**Example #7**

The frequency domain expression for the output over the input of a circuit is solved to be

$$\frac{\text{output}}{\text{input}} = \frac{10^5 (s + 5)}{(s + 1)(s + 5000)}$$

Substitute $s=j\omega$ into the above equation and calculate the magnitude (dB) and phase (degrees). Plug in values for $\omega$ equal to $10^1$, 0.8, 0.9, $10^{-1}$, 2, 3, 4, 5, 6, 7, $10^1$, $10^2$, $10^3$, 3000, 4000, 5000, 6000, 7000, $10^4$, $10^5$ rad/sec and plot these values on a semilog graph for both magnitude and phase. Recall that magnitude, $|a+bj| = \sqrt{a^2+b^2}$; and the phase, $\angle(a+bj) = \tan^{-1}(b/a)$

Magnitude:

$$\left| \frac{\text{output}}{\text{input}} \right| = \left| \frac{10^5 (j\omega+5)}{(j\omega+1)(j\omega+5000)} \right| = \frac{10^5 |(j\omega+5)|}{|(j\omega+1)||(j\omega+5000)|} = \frac{\sqrt{(10^5)^2 + 0^2 \sqrt{5^2 + \omega^2}}}{\sqrt{1^2 + \omega^2} * \sqrt{5000^2 + \omega^2}}$$

Phase:

$$\angle \left( \frac{\text{output}}{\text{input}} \right) = \angle \left( \frac{10^5 (j\omega+5)}{(j\omega+1)(j\omega+5000)} \right) = \angle 10^5 * \angle (j\omega+5)$$

$$\angle (j\omega+1) * \angle (j\omega+5000) = 0 + \tan^{-1} \left( \frac{\omega}{5} \right) - \tan^{-1} \left( \frac{\omega}{1} \right) - \tan^{-1} \left( \frac{\omega}{5000} \right) \ \{ @ \omega=0.1 \text{rad/sec} \Rightarrow \}$$

magnitude=99.5V/V=20*log(99.5V/V)=39.96dB; phase=0+1.15-5.7-0.001=-4.6 degrees
Bode Diagram

Frequency response
The "response" of a system or circuit is the output for a given input.

A "transfer function" is a mathematical description of how the output is related to the input.

\[
\text{output} = \text{Transfer function} \times \text{input}
\]

or...

\[
\text{Transfer function} = \frac{\text{output}}{\text{input}}
\]

No real system or circuit treats all frequencies the same, so all real transfer functions are functions of frequency.

Transfer function = \( H(\omega) \) or \( H(f) \) or, Transfer function = \( H(s) \)

The transfer function can be used to describe the "frequency response" of a circuit. That is, how does the circuit respond to inputs of different frequencies.

Bode Plots
- 2 plots – both have logarithm of frequency on x-axis
  - y-axis magnitude of transfer function, \( H(s) \), in dB
  - y-axis phase angle, in degrees

The plot can be used to interpret how the input affects the output in both magnitude and phase over frequency. To sketch the graphs, the circuit is first analyzed to find output/input (transfer function). This equation is used as the basis for the plots. The equation is analyzed for magnitude and phase as shown in the previous example (#5)
Is there a shortcut to graph the Bode plots?

**Magnitude Plot:**
1) Determine the Transfer Function of the system:

\[ H(s) = \frac{K(s + z_1)(s + z_2)\cdots}{(s + p_1)(s + p_2)\cdots} \]

2) Rewrite it by factoring both the numerator and denominator into the standard form

\[ H(s) = \frac{Kz_1z_2\cdots\left(\frac{s}{z_1} + 1\right)\left(\frac{s}{z_2} + 1\right)\cdots}{p_1p_2\cdots\left(\frac{s}{p_1} + 1\right)\left(\frac{s}{p_2} + 1\right)\cdots} \]

where the \( z \) s are called zeros and the \( p \) s are called poles.

3) Replace \( s \) with \( j\omega \). Then find the **Magnitude** of the Transfer Function.

\[ H(j\omega) = \frac{Kz_1z_2\cdots\left(\frac{j\omega}{z_1} + 1\right)\left(\frac{j\omega}{z_2} + 1\right)\cdots}{p_1p_2\cdots\left(\frac{j\omega}{p_1} + 1\right)\left(\frac{j\omega}{p_2} + 1\right)\cdots} \]

If we take the \( \log_{10} \) of this magnitude and multiply it by 20 it takes on the form of

\[ 20\log_{10}(H(j\omega)) = 20\log_{10}\left(\frac{Kz_1z_2\cdots\left(\frac{j\omega}{z_1} + 1\right)\left(\frac{j\omega}{z_2} + 1\right)\cdots}{p_1p_2\cdots\left(\frac{j\omega}{p_1} + 1\right)\left(\frac{j\omega}{p_2} + 1\right)\cdots}\right) = \]

\[ 20\log_{10}|K| + 20\log_{10}|z_1| + 20\log_{10}|z_2| + \cdots + 20\log_{10}\left|\frac{j\omega}{z_1} + 1\right| + 20\log_{10}\left|\frac{j\omega}{z_2} + 1\right| + \cdots - 20\log_{10}|p_1| - \cdots - 20\log_{10}\left|\frac{j\omega}{p_1} + 1\right| - 20\log_{10}\left|\frac{j\omega}{p_2} + 1\right| - \cdots \]

*Recall => \( \log(ab) = \log(a)+\log(b) \) and \( \log(a/b) = \log(a) - \log(b) \)*

You can see from this expression that each term contributes a number to the final value at a specific frequency. Therefore, each of these individual terms is very easy to show on a logarithmic plot. The entire Bode log magnitude plot is the result of the superposition of all the straight line terms. This means with a little practice, we can quickly sketch the effect of each term and quickly find the overall effect. To do this we have to understand the effect of the four different types of terms.

These include:
1) Constant terms \( K \)
2) Poles and Zeros at the origin \( 1, j\omega \)
3) Poles and Zeros not at the origin \( 1 + \frac{j\omega}{p_1}, 1 + \frac{j\omega}{z_1} \)
4) Complex Poles and Zeros (not addressed at this time)

**Effect of Constant Terms:**
Constant terms such as \( K \) contribute a straight horizontal line of magnitude 20 \( \log_{10}(K) \) (not dependent on frequency)
Effect of Individual Zeros and Poles at the origin:
A zero at the origin occurs when there is an $s$ or $j\omega$ multiplying the numerator. Each occurrence of this causes a positively sloped line passing through $\omega = 1$ with a rise of 20 dB over a decade.

$TF = \frac{j \omega}{1}$

If $\omega=0.1 \Rightarrow |j0.1| = 0.1V/V=20\log(0.1)=-20\text{dB}$
If $\omega=1 \Rightarrow |j1| = 1V/V=20\log(1)=0\text{dB}$
If $\omega=10 \Rightarrow |j10| = 10V/V=20\log(10)=20\text{dB}$

(\log scale)

A pole at the origin occurs when there are $s$ or $j\omega$ multiplying the denominator. Each occurrence of this causes a negatively sloped line passing through $\omega = 1$ with a drop of 20 dB over a decade.

$TF = \frac{1}{j \omega}$

If $\omega=0.1 \Rightarrow |\frac{1}{j0.1}| = 1V/V=20\log(10)=20\text{dB}$
If $\omega=1 \Rightarrow |\frac{1}{j1}| = 1V/V=20\log(1)=0\text{dB}$
If $\omega=10 \Rightarrow |\frac{1}{j10}| = 0.1V/V=20\log(0.1)=-20\text{dB}$

Effect of Individual Zeros and Poles Not at the Origin
Zeros and Poles not at the origin are indicated by the $(1+j\omega/z_i)$ and $(1+j\omega/p_i)$. The values $z_i$ and $p_i$ in each of these expression is called a break frequency. Below their break frequency these terms do not contribute to the log magnitude of the overall plot. Above the break frequency, they represent a ramp function of 20 dB per decade. Zeros give a positive slope. Poles produce a negative slope.

Before looking at the effect of the 2nd order terms, let’s learn how to plot with the three terms already described. We will work several examples where we show how the Bode log magnitude plot is sketched. To complete the log magnitude vs. frequency plot of a Bode diagram, superposition all the lines of the different terms on the same plot.

**Phase Plot:**
For our original transfer function,
the cumulative phase angle associated with this function are given by
\[ \angle H(j\omega) = \angle K\angle z_1\angle z_2 \cdots \angle \left( \frac{j\omega}{z_1} + 1 \right) \angle \left( \frac{j\omega}{z_2} + 1 \right) \cdots \angle p_1\angle p_2 \cdots \angle \left( \frac{j\omega}{p_1} + 1 \right) \angle \left( \frac{j\omega}{p_2} + 1 \right) \cdots \]

Then the cumulative phase angle as a function of the input frequency may be written as
\[ \angle H(j\omega) = \angle K + \angle \left[ z_1 + z_2 + \cdots - p_1 - p_2 - \cdots \right] + \tan^{-1}\left( \frac{w}{z_1} \right) + \tan^{-1}\left( \frac{w}{z_2} \right) + \cdots - \tan^{-1}\left( \frac{w}{p_1} \right) - \tan^{-1}\left( \frac{w}{p_2} \right) - \cdots \]

Once again, to show the phase plot of the Bode diagram, lines can be drawn for each of the different terms. Then the total effect may be found by superposition.

**Effect of Constants on Phase:**
A **positive** constant, \( K > 0 \), has no effect on phase. A **negative** constant, \( K < 0 \), will set up a phase shift of \( \pm 180^\circ \).

**Effect of Zeros at the origin on Phase Angle:**
Zeros at the origin, \( s \), cause a constant \(+90^\circ\) degree shift for each zero.

\[ \angle TF \]

<table>
<thead>
<tr>
<th>( \omega ) (log)</th>
<th>( j\omega = +90 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>+90 deg</td>
<td></td>
</tr>
</tbody>
</table>

**Effect of Poles at the origin on Phase Angle:**
Poles at the origin, \( s^{-1} \), cause a constant \(-90^\circ\) degree shift for each pole.

\[ \angle TF \]

<table>
<thead>
<tr>
<th>( \omega )</th>
<th>( \frac{1}{j\omega} = -90 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>-90 deg</td>
<td></td>
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</table>

**Effect of Zeros not at the origin on Phase Angle:**
Zeros not at the origin, like \( 1 + \frac{j\omega}{z_1} \), have no phase shift for frequencies **much lower** than \( z_1 \), have a \(+45^\circ\) deg shift at \( z_1 \), and have a \(+90^\circ\) deg shift for frequencies **much higher** than \( z_1 \).

\[ \angle TF \]

<table>
<thead>
<tr>
<th>( \omega )</th>
<th>( 0.1z_1 )</th>
<th>( z_1 )</th>
<th>( 10z_1 )</th>
<th>( 100z_1 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>+90 deg</td>
<td>+45 deg</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

To draw the lines for this type of term, the transition from \( 0^\circ \) to \(+90^\circ\) is drawn over 2 decades, starting at \( 0.1z_1 \) and ending at \( 10z_1 \).
Effect of Poles not at the origin on Phase Angle:

Poles not at the origin, like \( \frac{1}{1 + \frac{j \omega}{p_1}} \), have no phase shift for frequencies much lower than \( p_1 \), have a -45 deg shift at \( p_1 \), and have a -90 deg shift for frequencies much higher than \( p_1 \).

To draw the lines for this type of term, the transition from 0° to -90° is drawn over 2 decades, starting at 0.1\( p_1 \) and ending at 10\( p_1 \).

When drawing the phase angle shift for not-at-the-origin zeros and poles, first locate the break frequency of the zero or pole. Then start the transition 1 decade before, following a slope of ±45°/decade. Continue the transition until reaching the frequency one decade past the break frequency.

SUMMARY OF STRAIGHT-LINE APPROXIMATION PROCEDEUD STEPS (NO COMPLEX):

(Note that a decade is a multiple of 10 – 1, 10, 100, 1000, etc)

1. Rearrange the equation into standard form:

\[
H(s) = \frac{K z_1 z_2 \cdots \left( \frac{s}{z_1} + 1 \right) \left( \frac{s}{z_2} + 1 \right) \cdots}{p_1 p_2 \cdots \left( \frac{s}{p_1} + 1 \right) \left( \frac{s}{p_2} + 1 \right) \cdots}
\]

where \( K, z_1, z_2, \) etc are all constant values.

2. Determine the poles and zeros.

Note: If there are more than one poles/zeros at the same break frequency (say there are \( r \)), just multiply the slope/phase changes by \( r \). (ex. \( (1+s/10)^2 \) => it is a negative zero (numerator) and so it will change the slope by 2*20dB/dec and have a 2*45° slope/dec.

3. Draw the magnitude plot:

   a. Determine starting value:

   Case 1: No pole or zero at the origin:
   
   \[
   \text{starting value} = 20 \log_{10} \left( \frac{K z_1 z_2 \cdots}{p_1 p_2 \cdots} \right)
   \]

   Case 2: A pole or zero at the origin:

   - Pick a frequency value less than the lowest pole or zero value.
Plug in the frequency in the standard form equation above and take the magnitude. *This value is for that frequency only.* There is a constant slope going through this point. +20dB/dec slope if the location is a zero. -20dB/dec slope if the location is a pole.

b. Begin at the starting point. Start with the slope (0 slope if a constant, +20dB/dec slope if zero at origin, -20dB/dec slope if pole at origin). From left to right, at each zero add +20dB/dec to the current slope and at each pole -20dB/dec. Continue through each frequency.

4. Draw the phase plot:

a. Determine the starting value:

*Case 1: No pole or zero at the origin:*

If constant > 0 then starting value = 0°
If constant < 0 then starting value = ±180°

*Case 2: A pole or zero at the origin:*

starting value = +90° if zero at origin
starting value = -90° if pole at origin

b. Label each range of frequency according to the following (suggest putting on graph):

zero => from 1 decade before frequency to 1 decade after frequency: +45° slope/dec
pole => from 1 decade before frequency to 1 decade after frequency: -45° slope/dec
(eg if \(\omega = 10\) and is a pole then range is \(1 < \omega < 100\) with a slope of -45° slope/dec)

c. Look at each frequency range that has a slope. Add all slopes within that region. From left to right: start with starting value and slope of 0, continue until first region of change. Add all slopes within that region. Continue until the end is met. If no slope during a region the slope is constant (0).
**Example 8:** Sketch the Bode plots for \( H(s) = \frac{(s+100)(s+1k)}{(s+10)(s+10k)} \)
Example 9: Sketch the transfer function for \( H(s) = \frac{100(s + 100)(s + 10)}{(s^2)(s + 10k)} \)

Magnitude (2 poles at origin)
1. Determine start value: \((\omega = 1)\)
   \[ 20 \log \left( \frac{100(100)(10)}{10k} \right) = 20 \text{dB} \]
2. \(\omega = 10 \text{ (zero)} + 20 \text{dB/dec} \)
   \(\omega = 100 \text{ (zero)} + 20 \text{dB/dec} \)
   \(\omega = 10k \text{ (pole)} - 20 \text{dB/dec} \)

Phase (constant > 0 and 2 poles at origin)
1. Start Value: \(2 \times (-90^\circ) = -180^\circ \)
2. \(\omega = 10 \text{ (zero)}: \) \(1 < \omega < 100 + 45^\circ \text{ slope/dec} \)
\(\omega = 100 \text{ (zero)}: \) \(10 < \omega < 1k + 45^\circ \text{ slope/dec} \)
\(\omega = 10k \text{ (pole)}: \) \(1k < \omega < 100k - 45^\circ \text{ slope/dec} \)
Example #10 Bode Plots:

\[ \frac{V_c}{V_i} = \frac{4 \times 10^{-6} S}{30,200 \text{ mH s}^{-1} + 1} = \frac{(133n) \cdot S}{(2067n \cdot S + 1)} \]

Break frequency \( f = \frac{1}{\sqrt{2067n \cdot S + 1}} \) \( \Rightarrow \) \( s = \frac{1}{\sqrt{2067n \cdot S + 1}} = 3.75 \text{ MHz} \) with a zero at origin.

\[ \omega = 1 \Rightarrow 20 \log (133n) = -13.8 \text{ dB} \]

\[ \omega = 3.75 \text{ MHz} \Rightarrow 20 \log \left[ \frac{133n \times 3.75 \text{ MHz}}{\sqrt{(2067n \times 3.75 \text{ MHz})^2 + 1}} \right] = 20 \log (3.53) \approx -9 \text{ dB} \]

because of zero at origin: 90° phase shift at 3.75 MHz.

Note that this circuit only operates at frequencies above 375 rad/sec = 59 MHz.

Example 11:

Analyze the following circuit to find the transfer function \( \frac{V_i}{V_s} \). Solve the circuit symbolically first and then with their values. Sketch transfer function using a straight-line approximation procedure.

\[ \frac{V_i}{V_s} = \frac{R_1 || R_2 || \frac{1}{C_1}}{R_s + \left( R_1 || R_2 || \frac{1}{C_1} \right)} = \frac{R_i}{R_i + R_1 + \frac{1}{C_1}} \]

\[ \frac{V_i}{V_s} = \frac{R_i}{R_i + R_1 + \frac{1}{C_1}} = \frac{R_i}{R_i + R_1 + \frac{1}{C_1}} \cdot \frac{R_i + R_1 + \frac{1}{C_1}}{R_i + R_1 + \frac{1}{C_1}} = \frac{R_i (R_i + R_1 + \frac{1}{C_1})}{R_i + R_1 + \frac{1}{C_1}} \]

This circuit only operates above 200 kHz and below 2 MHz.
Amplifiers

**Purpose:** A weak signal is produced by a transducer (ex. Microphone) → too small for reliable processing, so amplify magnitude, i.e. make it larger.

Amplifier → basic element of analog circuits

- Batteries or power supplies are rarely shown on the schematic.
- Signal voltages are assumed to be referenced to ground even if the grounds aren't shown.

The output of all amplifiers are limited by the power supplies. Usually the limits are less than the power voltages.

**Output limits,** \( L^+ < V^+ \), \( L^- > V^- \) (usually)

The output can't go beyond these limits no matter what the input does. If you want to avoid the "clipping" distortion in the output, you have to limit the input (make sure it's within an acceptable range).

The transfer function has some non-linearities:

Often the clipping levels are not so well defined:

Many of the transistor amplifier circuits that we'll see this semester will have DC offsets and will invert the signal.

The signal is considered the AC (changing) part of the waveform and the DC is called "bias" or the "quiescent - point" (Q - point) of the circuit.
Gain

\[
\text{voltage gain } A_v = \frac{v_{out}}{v_{in}}
\]

lower-case letters refer to signal values

lower-case letters refer to signal values

\[
\text{current gain } A_i = \frac{i_{out}}{i_{in}} = \frac{i_L}{i_{in}}
\]

\[ \text{power gain } = \frac{P_{out}}{P_{in}} = \frac{P_L}{P_{in}} \]

DC: \( \frac{V_{OUT}}{V_{IN}} \) is rarely gain

Gains are dimensionless numbers

Gain is just an idealized transfer function.

If only 1 input is shown, assume that other input is grounded.

Two stages

\[
v_{in} \rightarrow A_{v1} \rightarrow v_{out1} \rightarrow A_{v2} \rightarrow v_{out} = v_{in} \cdot A_{v1} \cdot A_{v2}
\]

If \( A_{v1} = 10 \) \& \( A_{v2} = 4 \) then \( A_{total} = A_{v1} \cdot A_{v2} = 40 \)

Same holds for multiple stages

Multiple Stages

\[
v_{in} \rightarrow A_{v1} \rightarrow v_{out1} \rightarrow A_{v2} \rightarrow v_{out2} \rightarrow A_{v3} \rightarrow v_{out3}
\]

Gain expressed as ratios:

\[ A_{total} = A_{v1} \cdot A_{v2} \cdot A_{v3} \]

Gain expressed as dB:

\[ A_{total\,dB} = A_{v1\,dB} + A_{v2\,dB} + A_{v3\,dB} \]

If \( A_{v1} = 20 \), \( A_{v2} = 8 \) \& \( A_{v3} = 4 \) then \( A_{total} = A_{v1} \cdot A_{v2} \cdot A_{v3} = 640 \)

\[ A_{v1\,dB} = 20 - \log(20) \]
\[ A_{v2\,dB} = 20 - \log(8) \]
\[ A_{v3\,dB} = 20 - \log(4) \]

\[ 20\log(640) = 56.124 \, \text{dB} \]

Amplifier Models

Up until now we haven’t worried about the currents into and out-of our amplifiers. In reality, any source, including the amplifier, will have a source resistance (\( R_S \) or \( Z_s \) for the source and \( R_{out} \) or \( Z_{out} \) for the amp). Also any amplifier will let a little signal current flow in (modeled by an \( R_{in} \) or \( Z_{in} \)).

At this point, the triangle symbol gets to be a little cumbersome and is dropped.
Basic amplifier model:
Voltage amplifier with source and load

\[ V_{\text{out}} = \frac{V_{\text{in}}}{R_{\text{s}} + R_{\text{in}}} \cdot A_{\text{vo}} \cdot V_{\text{in}} \]

\[ V_{\text{out}} = \frac{V_{\text{in}}}{R_{\text{s}} + R_{\text{in}}} \cdot A_{\text{vo}} \cdot \frac{R_{\text{L}}}{R_{\text{o}} + R_{\text{L}}} \]

Overall gain:

\[ \frac{V_{\text{out}}}{V_{\text{s}}} = \frac{R_{\text{in}}}{R_{\text{s}} + R_{\text{in}}} \cdot A_{\text{vo}} \cdot \frac{R_{\text{L}}}{R_{\text{o}} + R_{\text{L}}} \]

or, in dB:

\[ 20 \log \left( \frac{V_{\text{out}}}{V_{\text{s}}} \right) = 20 \log \left( \frac{R_{\text{in}}}{R_{\text{s}} + R_{\text{in}}} \right) + 20 \log \left( A_{\text{vo}} \right) + 20 \log \left( \frac{R_{\text{L}}}{R_{\text{o}} + R_{\text{L}}} \right) \]

Three stage amplifier

Overall gain:

\[ \frac{V_{\text{out}}}{V_{\text{s}}} = \frac{R_{\text{in}1}}{R_{\text{s}} + R_{\text{in}1}} \cdot A_{\text{vo1}} \cdot \frac{R_{\text{in}2}}{R_{\text{o1}} + R_{\text{in}2}} \cdot A_{\text{vo2}} \cdot \frac{R_{\text{in}3}}{R_{\text{o2}} + R_{\text{in}3}} \cdot A_{\text{vo3}} \cdot \frac{R_{\text{L}}}{R_{\text{o3}} + R_{\text{L}}} \]

Desirable characteristics

Want \( R_{\text{in}} \to \infty \) High input resistance means the amplifier will not load down the source or previous stage.

Want \( R_{\text{L}} \to 0 \) Low output resistance means the amplifier supply lots of current to the load or next stage.

High \( R_{\text{in}} \) and low \( R_{\text{L}} \) means good current gain. In fact these terms are used much more often than "current gain".

At higher frequencies it may become more important to match impedances than to maximize \( R_{\text{in}} \) & minimize \( R_{\text{c}} \).

Other Amplifier Models

\[ i_{\text{in}} \quad R_{\text{i}} \quad \frac{v}{i} \quad \text{Transresistance amplifier} \]

\[ i_{\text{in}} \quad R_{\text{i}} \quad \text{Current amplifier} \]

\[ \frac{v}{i} \quad \text{Transconductance amplifier} \]

Instead of \( A_{\text{vc}} = \frac{v_{\text{o}}}{v_{\text{in}}} \) (unloaded)

This amp has \( R_{\text{m}} = \frac{v_{\text{o}}}{i_{\text{in}}} \) (unloaded)

\[ \frac{V}{I} = \Omega \], that's why it's called transresistance

Instead of \( A_{\text{vo}} = \frac{v_{\text{o}}}{v_{\text{in}}} \) (unloaded)

This amp has \( G_{\text{m}} = \frac{i_{\text{o}}}{v_{\text{in}}} \) (unloaded)

\[ \frac{1}{V} = \text{conductance, that's why it's called transconductance, units mho or seimen} \]
Procedure for solving ideal op-amp circuits:
1. If the noninverting terminal of the op-amp is at ground potential, then the inverting terminal is at virtual ground. Sum currents at this node, assuming zero current enters the op-amp itself.
2. If the noninverting terminal of the op-amp is not at ground potential, then the inverting terminal voltage is equal to that at the noninverting terminal. Sum currents at the inverting terminal node, assuming zero current enters the op-amp itself.
3. For the ideal op-amp circuit, the output voltage is determined from either step 1 or step 2 above and is independent of any load connected to the output terminal.

Example 12:
For the circuit below, assume an ideal op-amp. Find the currents through all branches and the voltages at all nodes. Since the current supplied by the op amp is greater than the current drawn from the input signal source, where does the additional current come from?

\[ V_0 = \frac{I_1}{5k} = \frac{5V + 0.2\sin(10t)}{5k} \]

\[ I_1 = I_2 = \text{mA} + 40\mu\text{A}(\sin(10t)) \]

\[ V_0 = -I_2 (200k) \]

\[ V_0 = -200V - 80\sin(10t) \]
Example 13: Use the following circuit.

![Circuit Diagram]

You are given:  Amp₁ has an \(A_{vo}=5\), \(R_i=500\), \(R_o=12k\)  Amp₂ has an \(A_{vo}=20\), \(R_i=3k\), \(R_o=4k\)

(a) Find \(A_v= \frac{V_L}{V_s}\) Express your answer as a ratio in dB.

(b) Evaluate the overall current gain \(\frac{i_L}{i_s}\). Express your answer as a ratio and in dB form.

(c) Evaluate the overall power gain \(\frac{P_L}{P_s}\). Express your answer as a ratio and in dB form.

(d) If \(V_s=40mV_{pp}\). What is the output voltage (peak-to-peak) at \(V_L\)?

(e) What value would \(R_o\) for Amp₂ need to be changed in order to get \(A_v = 4\)?
Operational Amplifier:

An operational amplifier is basically a complete high-gain voltage amplifier in a small package. Op-amps were originally developed to perform mathematical operations in analog computers, hence the odd name. With the proper external components, the operational amplifier can perform a wide variety of operations on the input voltage. It can multiply the input voltage by nearly any constant factor, positive or negative, it can add the input voltage to other input voltages, and it can integrate or differentiate the input voltage. The respective circuits are called amplifiers, summers, integrators, and differentiators. Op-amps are also used to make active frequency filters, current-to-voltage converters, voltage-to-current converters, current amplifiers, voltage comparators, etc. etc. These little parts are so versatile, useful, handy, and cheap that they’re kind of like electronic Lego blocks — although somewhat drably colored.

Op-amp characteristics
An op-amp has two inputs
Amplifies the voltage difference between those two inputs.

\[ v_o = G(v_a - v_b) \]

- **noninverting input**
  - \( v_o \)
  - \( v_i \)
- **inverting input**
  - \( v_o \)
  - \( -v_i \)

\( G = \text{voltage gain of the op-amp} \)
\( G \) is usually very big, \( > 100,000 \)

The op-amp must be connected to external sources of power, \( V^+ \) and \( V^- \).

The output voltage is limited by the power supply voltages.

\[ -V^- \leq v_o \leq V^+ \]

(Usually even more limited than this)

So: \( V^- \leq G(v_a - v_b) \leq V^+ \)

If the op amp is in its **active region**:
Since \( G \) is very big, \( (v_a - v_b) \) must be very small, in fact the usual assumption is that

\[ v_o \approx v_a \]

Active region ONLY

**Op Amp Configurations:**

1. **Voltage Follower** => \( V_o = V_i \)

   Used as a **current amplifier**

2. **Noninverting amplifier** =>

   \[ v_o = \left( \frac{R_2}{R_1} + 1 \right) \cdot v_i \]

3. **Inverting amplifier** =>

   \[ v_o = -\frac{R_2}{R_1} \cdot v_i \]

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4. **Summer** =>

\[ v_o = \left( \frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3 + \cdots + \frac{R_f}{R_n} v_n \right) \]

5. **Differential Amplifier** =>

\[ v_o = \left( \frac{R_2}{R_1} (v_2 - v_1) \right) \]

6. **Instrumentation Amplifier** =>

   * This amplifier configuration can have large gain because of the two stages. Lower noise. Typically used for sensors output amplification where the signal is very small.

\[ v_o = \left( \frac{R_2}{R_1} (v_2 - v_1) \right) \]

**Internally Compensated Op Amp**

This is the open-loop gain \((A)\) of a LM741 (worst case). Usually \(f_t\) and \(f_b\) are a little higher than those shown here, especially in better quality op-amps. You probably measured \(f_b\), somewhere between 1 & 2 MHz in the lab, even for a 741. They normally exceed their specifications a little.

\[ A = \frac{A_0}{1 + j \frac{f}{f_b}} \]

**Other symbols for \(f_b\):** \(f_r, f_u, f_{\text{unity}}, GB, \text{Bandwidth}\)

**A (open-loop) gain**

\[ f_b = \text{gain-bandwidth product} \]

\[ f_t = \text{unity-gain bandwidth} \]
Closed-loop (with negative feedback) Frequency Response

If your op-amp circuit is designed to have a gain of 100 (40dB) then a very good estimate of its frequency response is shown at right. To find the bandwidth of your amplifier, you take the gain-bandwidth product \((f_b)\) and divide by the gain of your amp.

\[
f_c \approx \frac{\Lambda_o f_b}{G} = \frac{f_t}{G}
\]

\(G = \text{ideal gain of amplifier}\)

If you plug \(A = \frac{f_t}{j\pi f} \) into the finite-gain equations on the last page, you'll find that this estimate is exact for a noninverting amplifier, but not quite right for an inverting amplifier.

\[
f_c \approx \frac{\Lambda_o f_b}{G} = \frac{f_t}{G} = \frac{f_t}{1 + \frac{R_f}{R_i}}
\]

If \(G > 20\) or so, you can usually neglect the +1 in the denominator.
Use the attached datasheet information. Amp1 is a CA3140 and Amp2 is an LM741.

(a) State each amplifiers frequency response transfer function (V_i/V_{in} and V_o/V_i)
(b) State the overall transfer function (V_o/V_{in})
(c) Write the equation to solve for the overall f_{3dB} of the circuit below. {Note you do not need to solve it}

a) Amp 1 ⇒ \( \frac{V_i}{V_{in}} = \frac{-20}{(1+\frac{jF}{20k})} \)

\( f_{3dB} = \frac{4MHz = 200k}{(20)} \)  only for Amp1

Amp2 ⇒ \( \frac{V_o}{V_i} = \frac{1M}{(30)} = 33.3k \)

\( \frac{V_o}{V_i} = \frac{-33.3k}{(1+j\frac{F}{33.3k})} \)

b) \( \frac{V_o}{V_{in}} = \frac{-20}{(1+j\frac{F}{200k}) (1+j\frac{F}{33.3k})} \)

\( 426.6V/V \) (52.6dB)

600dB ⇒ 20log(600) = 55.6dB
55.6dB - 3dB = 52.6dB
52.6dB = \( \frac{52.6}{10.20} = 4.06 \) V/V

\( 426.6 = \frac{600}{\sqrt{1^2 + \left(\frac{f_{3dB}}{200k}\right)^2}} \)
Op Amps output voltage can only change so fast. The maximum rate of change is called slew rate (SR)

**Slew Rate continued**

A square wave or a step function can be approximated by a sine wave. The idea is to determine the maximum slope of the output versus input. The maximum slope must be less than the slew rate, so:

\[
\frac{V_o}{V_{in}} = \frac{-R_2}{R_1} \quad (R_1 \ll V_{os})
\]

\[
R_1 \ll \frac{1}{C_s} = \left(\frac{R_1(\frac{1}{C_s})}{R_1} + \frac{1}{C_s}\right) = \frac{R_1}{(R_1C_s + 1)}
\]

\[
V_{in} = \frac{-R_2 (R_1C_s + 1)}{R_1}
\]

**DC Imperfections:**

**Offset Voltage (Vos)** The voltage for the output below should be zero, but almost always is not. The value when both inputs are grounded is called the voltage offset, Vos. To compensate for this offset =>

- a fixed voltage can be placed at the input as shown below. Several op amps have an extra terminal in the package (offset null terminal) that can be adjusted so that the output will read zero when the inputs are both grounded. This value is also affected by temperature and so can not always be compensated.

**Input bias currents (I_{B1}, I_{B2}, \text{ave}=I_B)** The real op amp has currents as seen below. \((V_o=I_B R_f)\)

**The cure if \(I_{B1}=I_{B2}\):**

- if \(v_o = 0\)
- \(v_b = (R_1 || R_{in}) I_{B1}\)
- if \(R_{in} = (R_1 || R_{in}) I_{B2}\)
- then \(v_a = (R_1 || R_{in}) I_{B2}\)

So: maxo \(R_1 = |R_1 || R_{in}|\)

To reduce input bias current => match impedances seen at each terminal to be the same.
Op Amp Imperfections Summary:
1. Clipping
   Increase DC voltage supply (increases power consumption)
   Decrease input signal
2. Slew Rate
   \[ f_{\text{max}} = \frac{\Delta V}{V_p 2\pi} = \frac{\Delta V}{V_{pp} \pi} \]
3. Voltage offset
   Use external voltage source to compensate
4. Input Bias Current
   Match impedances at both inputs

Example 16:
You are given the following characteristics for a real amplifier along with the circuit below.

\[ V_{io} = 4.0 \text{mV} \quad A_o = 100 \text{dB} \]
\[ I_{io} = 200 \text{nA} \quad f_T = 2 \text{MHz} \]
\[ I_{ib} = 600 \text{nA} \quad V_{\text{swing}} = \pm 15 \text{V} \]
\[ R_i = 1 \text{M}\Omega \quad \text{slew rate} = 4 \text{V/\mu s} \]
\[ R_o = 50 \Omega \]

(a) What is the voltage gain of the circuit? Ignore Ri and Ro and only consider the finite gain, A_o.
(b) For small input signals, what is the 3db bandwidth of the circuit (in Hz)?
(c) For an output signal of 10Vpp, considering the slew rate effect, what is the limiting frequency of the circuit?
(d) What is the maximum peak-to-peak output you can get without clipping?
(e) Find the effect of the input offset voltage (v_{in} = 0V), (i.e. find output value when input = 0)
(f) How should the circuit be modified to minimize the effect of the input bias current? Show the modification on the schematic above and find the value of any added parts.
What are diodes?

Definition: A diode is a semiconductor device that passes current only in 1 direction. A “one-way” current valve

Ideal Diode
Circuit Symbol:

- Like resistors, they have 2 terminals
Unlike resistors which have a linear relationship, the diode has a nonlinear characteristic.

**Reverse Bias:**
- Anode: $i = 0$
- Cathode: $v_D = \text{open}

**Forward Bias:**
- Anode: $i > 0$
- Cathode: $v_D = \text{open}

External circuit – needs to limit the forward current through a diode that is ON and limit the reverse voltage across a diode that is CUTOFF. Let’s look at some examples of diodes in a circuit.

**Summary of 2 modes of operation for Diode:**

<table>
<thead>
<tr>
<th>Forward-Biased</th>
<th>Reverse-Biased</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conducting (ON)</td>
<td>Cutoff (OFF)</td>
</tr>
<tr>
<td>Short Circuit</td>
<td>Open Circuit</td>
</tr>
<tr>
<td>$i=\text{value}, v_D=0$</td>
<td>$i=\text{none}, v_D=\text{open}$</td>
</tr>
</tbody>
</table>
Example: Rectifier

- The word “rectify” means to make unidirectional \(\rightarrow\) keep this in mind
- Makes use of nonlinear characteristic of diodes
- Assume ideal diode

1). Circuit:

```
V_s
```

2). Input signal \(V_s\): sinusoid

Two regions to consider:

3). \(V_s > 0\) – Will diode be conducting or cutoff? Conducting because current flows through diode in its forward direction (or look at inconsistency if you assume cutoff)

```
Vs
```

Voltage across R is then just \(V_s\)

4). \(V_s \leq 0\) – Will diode be conducting or cutoff? Cutoff (this is consistent)

```
I=0
```

no current \(\rightarrow\) \(V_o = 0\)

5). Output signal:

```
Vs
```

6). Used to convert ac \(\rightarrow\) dc \(\rightarrow\) \(V_s\) is ac with 0 average value. Can see \(V_o\) has a dc component.

\(t\)
Example 17: Two diodes

Find I and V. Assume the diodes are ideal. Not always obvious if diodes are ON or OFF → make an assumption and test it! Assume both are ON for starters → Short them

\[ V_B = 0 \]
\[ V = 0 \]
\[ I_{D2} = \frac{10 - 0}{5k} = 2\text{mA} \]
\[ I = \frac{-10}{10k} = 1\text{mA} \]
\[ I_{D1} + I_{D2} = I \Rightarrow I_{D1} = -I_{D2} = -2\text{mA} + 1\text{mA} = -1\text{mA} \]

Is this possible?
Diode ON: Need I>0 for V=0

We have V = 0, but I < 0 → contradiction
(Also think of it as saying a negative current is flowing through D1 → not possible)

Instead, say D1 is OFF and D2 is ON. Then \[ I_{D2} = \frac{10 - (-10)}{15k} = 1.33\text{mA} \]

Voltage at B: \[ V = V_B = -10 + 10k(1.33\text{mA}) = 3.3\text{V} \]

I = 0 and D1 is Reverse-biased
Is this consistent?

check:

D1: \[ I_{D1} = 0 \]
\[ 0V + v_{D1} - 3.3V \]
\[ v_{D1} = -3.3V < 0 \Rightarrow I_{D1} = 0 \]

D2: \[ I_{D2} = 1.33\text{mA} \]
\[ 10V + v_{D2} - 3.3V \]
\[ I_{D2} > 0 \Rightarrow v_{D2} = 0 \]

Think of finding I and V like solving a puzzle…
**Method for analyzing diode circuit:**

1. Assume each diode is either ON or OFF
2. Find $i_d$ and $v_d$ for each diode to see:
   - Is solution consistent with
     - OFF: $v_D \leq 0$ (ideal) or $v_D \leq v_{DO}$ (real) $\Rightarrow I_D = 0$
     - ON: $I_D > 0 \Rightarrow v_D = 0$ (ideal) or $v_D = v_{DO}$ (real)

*Make sure you are looking at voltage across the diode and current through the diode when you are checking for this! NOT the I and V necessarily that you were asked to find.*

3. If so, assumption was correct (check consistency) – only one solution possible, so STOP
4. Find the requested I and/or V
5. If not, start again with new assumption (NOTE: I and V values are no longer valid, so you have to discard those previous values)

---

**Example 18**

*Find I and Vo*

Assume “ON”:
- $V_0 = -5V$
- $I = \frac{5-(-5)}{5k} = 2mA$

**check:**
- $I_D > 0 \Rightarrow v_D = 0$

---

Assume both “ON”:
- $V_0 = -10V$
- $I = \frac{0-(-10)}{1k} = 10mA$

**check:**
- $I_D > 0 \Rightarrow v_D = 0$
Analysis of Diode Circuits
For hand calculations, we have 4 main models to use:

1). Ideal model for diode:
   - Reverse Bias: OFF/cutoff/open circuit
   - Forward Bias: ON/conducting/short circuit

2). Use full diode equation: \( i_D = I_S (e^{V_D/nV_T} - 1) \)
   - (Reverse Bias: \( i_D \approx -I_S \))
   - Forward Bias: \( i_D \approx I_S (e^{V_D/nV_T} ) \)
   - Use an iterative method and solve

3). Constant-voltage-drop model for diode (apply for forward bias):
   - Replace real diode with an ideal diode and a voltage drop \( V_D \)

4). Piecewise-linear model for diode (apply for FB):
   - Replace real diode with an ideal diode, a voltage drop \( V_{D0} \), and a resistor, \( r_D \)
Example 19:
Assume all diodes are identical and have $V_{BD}=0.7V$, $n=1$, and $V_T=25mV$. Use the constant voltage drop method. Verify that your assumption for the diode operation (i.e. on or off) are correct. Find the following making sure you find the correct operation of the diodes.

a) State your assumptions (diode is on/off).
b) The current $I_D$
c) The current $I_{D2}$
d) The voltage $V_o$
e) Your verification to prove your assumptions for the diodes are correct.

- $D_1$ on, $D_2$ off ($D_2$ will have $-3V$ across it from observation: voltage polarity is wrong direction).

$b)$ $I_{D1} = \frac{11.3}{1k} = 11.3mA > 0$

- $I_{D2} = 0$
- $V_o = -3V$
- $-3V - V_{D2} = 0 \Rightarrow V_{D2} = -3V < 0$
- Assumption $D_2$ on correct.

$D_1$ and $D_2$ on $\Rightarrow$

- $I_{D1} = \frac{11.3}{1k} = 11.3mA$
- $V_{D2} = \frac{-3}{3.7k} = -1mA < 0$

$D_2$ on, $D_1$ off $\Rightarrow$

- $I_{D2} = \frac{-3.7}{3.7k} = -1mA < 0$

Dr. Rasmussen
Small-Signal Analysis of Diodes

- So far we have looked at dc models for diodes
- For some applications it is necessary to also use a "small-signal" ac model
- If we use a small-signal model that linearizes the components, we can apply regular linear circuit analysis!
- We can then separate ac and dc analysis

The technique used to linearize a nonlinear characteristic is called biasing.

Biasing:

- Biasing is achieved by operating the circuit with the nonlinear characteristic in a point near the middle
- From the graph, at dc voltage input \( V_i \) the dc voltage output is \( V_o \).
- The point \( Q \) is known as the quiescent point, the dc bias point, or the operating point
- By limiting the amplitude of a ac time varying input signal, \( v_i(t) \) the operating point is limited to a linear region of the curve.
- Note that this only works when the input signal is kept sufficiently small

Derivation of the small-signal is done in the book (pg. 160).

The meaning of CAPITALS and lower case letters

<table>
<thead>
<tr>
<th>examples</th>
<th>meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_D )</td>
<td>DC, Bias quantity</td>
</tr>
<tr>
<td>( i_D )</td>
<td>AC, signal</td>
</tr>
<tr>
<td>( V_{D0} )</td>
<td>DC and AC together</td>
</tr>
</tbody>
</table>

- Hard to analyze circuit with both signals together
  - Result of derivation: Can separate analysis into DC then AC!
  - \( r_d = nV_T/I_D = \) small-signal resistance \{result of analysis\}

**NOTE:** This \( r_d \) is different than \( r_D \) from dc model

This \( r_d \) comes into play as the slope of the line tangent to the operating point:

\[
\text{slope} = \frac{1}{r_d}
\]

Equivalent circuit model for the diode for small changes around the operating point:

\[
v_D = V_{D0} + i_Dr_d = V_{D0} + (I_D + i_d)r_d = (V_{D0} + I_Dr_d) + i_d r_d = V_D + i_d r_d (DC + AC)
\]
**Procedure:**

1. Do dc analysis first (what we have done so far) to find $I_D$
2. Use dc current value ($I_D$) to determine small-signal model parameter $r_d = nV_T/I_D$
3. Then do ac analysis to find $i_d$ and $v_d$ (AC values)

**Example: Voltage Regulation** – given an ac input voltage, provides = constant dc voltage at output

Circuit:

- $V_{DD}=10V$
- $v_s=\sin(2\pi 60t)$
- Assume diode has 0.7V drop at 1mA and $n=2$
- $V_D=0.7V$

1. First perform **dc analysis** using constant voltage drop model - dc circuit model:

$$-V_{DD} + I_D(R) + V_{D0} = 0$$

$$I_D = (10-0.7)/5k = 1.86mA$$

2. Calculate small-signal resistance (depends on dc current!): $r_d = nV_T/I_D = 2(25mV)/1.86m = 26.8\, \Omega$

3. Perform **ac analysis** using small-signal model small-signal circuit model:

$$v_s + i_d(R+r_d) = 0 \Rightarrow i_d = v_s/(R+r_d)$$

$$v_d(\text{peak-to-peak}) = i_d(r_d) = \frac{v_s r_d}{(R+r_d)} = \frac{2(26.8)}{(5k+26.8)} = 10.7mV$$

Input: $10V_{dc} + 2V_{pp} \text{ ac} \Rightarrow \text{i.e. ac is 10\% of dc}$

Output: $0.7V_{dc} + 10.7mV_{pp} \text{ ac} \Rightarrow \text{ac is } \approx 0.8\% \text{ of dc}$

**Physics of Diode**

A diode is made up of what is called a pn-junction.

*What is one main characteristic of a metal?* Metals: tend to be good conductors because they have “free electrons” that can move easily between atoms; *flow of electrons* → *current flow*

*Insulators:* electrons in covalent bonds, so they can’t move around; no flow of electrons → no current flow

A pn-junction has two different pieces of silicon (between a metal and insulator) that when put together and applying a forward voltage of approximately > 0.7V, we will have a conducting device that has current flow through it fully in one direction and very minutely in the reverse direction → You can change the behavior of silicon by *doping* it

**Doping:** mix small amount of impurities into the silicon which changes its charge


**Silicon atoms**

Silicon atoms each have 4 valence electrons (electrons in their outermost shell). That leaves 4 spaces in the outer shell of Si. This makes silicon a very reactive chemical, like carbon, which has the same valence configuration.

**Silicon crystals**

Each atom covalently bonds with four neighboring atoms to form a tetrahedral crystal, which we’ll represent in 2D.

---

**Two types:**

**p-type**

- $n_{p0}$: concentration of free electrons in p-type
- $p_{p0}$: concentration of holes in p-type
- $N_A$: concentration of acceptor atoms

- p-type silicon ~ **Positive** charge
  - {holes are **majority**}

- $P_{p0} \equiv N_A \rightarrow n_{p0} \equiv \frac{n_{p0}^2}{N_A}$

- $n_{p0}$ is a function of temperature, $p_{p0}$ independent of temperature

- A **diffusion current** $I_D$ results in the forward

- **Minority carriers** drift: Thermally generated holes in n material (electrons in p material) diffuse to edge of depletion region $\rightarrow$ electric field causes them to be swept across to the p side (n side)

$\rightarrow$ **Drift current** $I_S$ is due to **minority carriers** diffusion (Temperature dependent since minority carriers are thermally generated)

If no external current/voltage is applied, the above two currents will be equal:

$I_D = I_S$ (Note: Can say diode current is $I_D = I_D = I_S = 0$)

The built-in voltage, $V_O$, keeps this equilibrium.

There is a “**built-in** voltage ($V_O$) across the depletion region – acts as a barrier that diffusing holes or electrons have to overcome $\rightarrow$ larger it is $\rightarrow$ harder to overcome $\rightarrow$ fewer carriers diffuse $\rightarrow$ smaller $I_D$

**Summary:** electrons and holes have high mobility and result in current flow with applied current or voltage

---

Dr. Rasmussen  
Spring 2011
It turns out that the free carriers are the most important things in the semiconductor crystals, so we can simplify the drawings to show only these free carriers.

**PN Junction**

When a p-type semiconductor is created next to an n-type, some of the free electrons from the n side will cross over and fill some of the free holes on the p side. This makes the p side negatively charged and leaves the n side positively charged. When the voltage across the junction reaches about 0.7 V the electrons find it too difficult to move against the charge and the process stops.

A region near the junction is now depleted of carriers and (surprise) is called the depletion region.

**Reverse bias**

This pn junction is now a diode. If you place an external voltage across the diode in the reverse bias direction, the depletion region gets bigger and no current flows.

This reverse bias region can be can be used as a heat or light sensor since the only current flow should be due to a few carriers produced by these effects.

The reverse biased diode can also be used as a voltage variable capacitor since it is essentially an insulator (the depletion region) sandwiched between two conducting regions.

**Forward bias**

If you place an external voltage across the diode in the forward bias direction, the depletion region shrinks until your external voltage reaches about 0.7 V. After that the diode conducts freely.
MOSFET

- This type of device dominates Integrated Circuit (IC) development due to their small size and low power consumption.
- These devices have a totally different operating mechanism than BJT but once biased and linearized to allow linear small-signal operation, the same small-signal model for the BJT are applicable with little modifications.
- Structure of MOSFET: A 4-terminal device.

Threshold Voltage

Need some minimum voltage to induce a channel (n) in the p substrate.

This minimum voltage is $V_t$, the threshold voltage. Usually, $1 V < V_t < 3 V$ but is very variable (like β).

Below this voltage the FET is off.

Characteristics:
- 3 regions of operation:
  - cutoff
  - triode: $|V_{DS}| \leq |V_{GS} - V_t| \cdot 1, V_{GS} > V_t$
    \[ i_D = k_n \frac{W}{L} (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \]
  - saturation: $|V_{DS}| \geq |V_{GS} - V_t| \cdot 1, V_{GS} > V_t$
    \[ i_D = \frac{1}{2} k_n \frac{W}{L} (V_{GS} - V_t)^2 \]

$k'_n = \text{process transconductance parameter} = 20 \text{ to } 100 \ \mu A/V^2$

$W = \text{channel width}$

$k'_p = 8 \text{ to } 40 \ \mu A/V^2$

$L = \text{channel length}$

$K = k'_n \frac{W}{L} = \text{gain factor (combined in books that are less interested in IC design)}$

$k'_n = \mu_n C_{ox}$
$\mu_n = \text{electron mobility} = 580 \text{ cm}^2/\text{V.s}$
$\mu_p : = 230 \text{ cm}^2/\text{V.s} \approx 40\% \mu_n$

$C_{ox} = \frac{\text{oxide capacitance}}{\text{unit area}} = \varepsilon_{ox} k_{ox} = \text{permittivity/thickness} = \text{capacitance/unit area}$
Characteristic Curves

**Triode region** (a.k.a., ohmic or linear)
- $V_{DS} < V_{GS} - V_t$
- $V_{GD} > V_t$
- $V_{DS} = V_{GS} - V_t$
- $V_{GD} = V_t$

**Saturation region** (a.k.a., constant current or active)
- $V_{DS} > V_{GS} - V_t$
- $V_{GD} < V_t$
- $i_D \approx \frac{1}{2} k' n' L (V_{GS} - V_t)^2$

Curve bends because the channel resistance increases with $V_{GS}$

Almost a straight line with slope proportional to $(V_{GS} - V_t)$

Current saturates because the channel is pinched off at the drain end, and $V_{GS}$ no longer affects the channel.

$V_{GS} > V_t$

Representative $V_{GS}$ values
- $V_{GS} = 8V$
- $V_{GS} = 7V$
- $V_{GS} = 6V$
- $V_{GS} = 5V$
- $V_{GS} = 4V$
- $V_{GS} = 3V$

$V_t \sim 2V$

Representative $i_D$ vs $V_{DS}$ curves
Early effect, channel length modulation \( (r_o) \)

However, the pinched-off spot does get bigger as \( V_{DS} \) increases, leading to a shortening of the rest of the channel, and correspondingly more current. This leads to "channel length modulation" which is just like base width modulation in the BJT. It also leads to an Early voltage, sloping lines in the saturation region, and an output resistance.

\[
i_D = \frac{1}{2} k' \frac{W}{L} (V_{GS} - V_t)^2 \left( 1 + \frac{r}{V_{DS}} \right)
\]

\[
\lambda = \frac{1}{V_A}
\]

\[
r_o = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{\lambda} \frac{1}{2} k' \frac{W}{L} (V_{GS} - V_t)^2
\]

Example

- Cross-Section

Source \((1.599)\)

Gate \((3.33V)\)

Drain \((7.335)\)

Induced channel – current flows from drain to source

\[
K' = \frac{2mA}{V^2}, \quad I_D = \frac{1}{2} (3m)(V_{GS} - V_t)^2
\]

\[
V_S = 2: \quad I_D = 1.5m
\]

\[
V_{GS} = 3: \quad I_D = 6m
\]

Symbols:

n-channel enhancement:
Example 19: Let $I_D=0.4\, \text{mA}$, $V_D=+1\, \text{V}$

Given: $V_t=2\, \text{V}$, $\mu_n C_{ox}=20\, \mu\text{A/V}^2$, $L=10\, \mu\text{m}$ and $W=400\, \mu\text{m}$ \left(\frac{W}{L}\right)=40$

Assume SATURATION: $I_D \propto V_{GS} \left( \lambda = 0 \right)$

$$I_D = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_t)^2$$

$$0.4 \times 10^{-3} = \left( \frac{1}{2} \right) 20 \times 10^{-6} (40)(V_{GS} - 2)^2$$

$$0.4 \times 10^{-3} = 400 \times 10^{-6} (V_{GS}^2 - 4V_{GS} + 4)$$

Quadratic Solution: $ax^2+bx+c \Rightarrow x = \frac{-b \pm \sqrt{b^2-4ac}}{2a}$ (2 solutions)

Therefore, $V_{GS} = \frac{4 \pm \sqrt{16 - 4(1)(3)}}{2} = 4 \pm \sqrt{1} = 1$ or $3\, \text{V}$

Since $V_t=2\, \text{V}$ then $V_{GS}=1\, \text{V}$ does not have the transistor on so $V_{GS}=V_G-V_S=3\, \text{V}$ and so $V_S=-3\, \text{V}$

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-3 - (-5)}{0.4} = 5\, \text{k}\Omega$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5 - 1}{0.4} = 10\, \text{k}\Omega$$
Example 20:
Solve the circuits below to find \( V_G \), \( V_D \), and \( V_S \). Find the currents in all branches. Assume \( \lambda = 0 \) and \( |V_t| = 1 \), \( k_n'(W/L) = 100 \mu A/V^2 \).

\( I_G = 0 \) \( V_G = +5V \) \( V_S = I_D(1k) \) \( V_D = 10 - I_D(500) \)

\[ I_D = \frac{1}{2} k_n' \left( \frac{W}{L} \right) (V_{GS} - V_t)^2 (1 + \lambda V_{DS}) \]

Assume Sat:
\[ I_D = \frac{1}{2} (100 \times 10^{-6}) (5 - I_D(1k) - 1)^2 (1 + 0(V_{DS})) \]
\[ 0 = 8 \times 10^{-4} - 1.4I_D + 50I_D^2 \]
\[ I_D = \frac{1.4 \pm \sqrt{(-1.4)^2 - 4(50)(8 \times 10^{-4})}}{2(50)} = 0.584 mA, 0.0274 \]

\( I_D = 0.0274 \):
\( V_S = 27.4V \Rightarrow V_{gs} < V_t \) (OFF!)

\( I_D = 0.584mA \):
\( V_S = 0.584V \) \( V_D = 9.71V \) \( V_{DS} = 9.12 > 3.416 = (V_{gs} - V_t) \) (SAT.)

Transconductance

\[ i_D = \frac{1}{2} k_n' \left( \frac{W}{L} \right) (V_{GS} - V_t)^2 \]

\[ \text{Slope} = \frac{d}{dv_{GS}} I_D = \frac{d}{dv_{GS}} \left[ \frac{1}{2} k_n' \left( \frac{W}{L} \right) (V_{GS} - V_t)^2 \right] \]
\[ = \left[ k_n' \left( \frac{W}{L} \right) (V_{GS} - V_t) \right] \cdot 1 = \frac{i_d}{v_{gs}} \text{ small signal values} \]

Also called "transfer admittance, \( y' \)"

Use \( \frac{1}{g_m} \) in gain equations like \( r_c \) for BJT's

Small-signal model:

**hybrid-\( \pi \) (use when there is not a resistor in the source)**

\[ r_o = \frac{V_A}{I_C} \approx \frac{1}{\lambda I_C} \]

ignore if large

**model-T (use when there is a resistor in the source - makes analysis a little easier)**
Example 20 (4.8 from book)

\( k'(W/L) = 1 \text{mA/V}^2 \), \( V_T = 1 \text{V} \), \( R_D = 18 \text{kohm} \), \( V_{DD} = 10 \text{V} \)

Find a good Q-point (bias point) to operate the amplifier.

\[ V_{GS} = V_{DS} \]

\[ V_{OC} = V_{BB} = V_T \]

\[ V_{DD} = V_{DS} \]

Dr. Rasmussen
Biasing of MOSFET:
- Biasing is a key step in transistor design. It puts the transistor configuration at a good point in the saturation region that ensures that $I_D$, $V_{OV}$, and $V_{DS}$ are predictable and stable and do not vary by a large amount when the transistor is replaced by another of the same type.
- $R_G$ can be made very large: high $R_{in}$
- We need $R_S$ to stabilize $I_D$ from variations in $V_t$
- For IC (integrated circuit) design, we use active biasing or a constant current source.
  - Minimize number or $R$’s and caps on an IC due to their large area requirement
    - Use active load for $R$
    - Use direct coupling for $C$

Current source bias from current mirror

Most common bias in ICs involves a current source.

Current mirrors

$$I_{D1} = \frac{1}{2} k' n \frac{W}{L} (V_{GS} - V_t)^2$$

The same $V_{GS}$ can be used to turn on many current sources, each with its own $W/L$ ratio.

Example 21

$I_{REF}=100\mu A$, $Q_1$ & $Q_2$ same: $(W/L)=(100\mu m/10\mu m)$, $V_t=1V$, $k' n=20\mu A/V^2$, $V_A=10L$

$I_o=100 \mu A$

$$I_{D1} = I_{REF} = 100 \mu A = \frac{1}{2} 20 \mu A (10) (V_{GS} - 1)^2$$

$$100 \mu A = 100 \mu A (V_{GS} - 1)^2 \Rightarrow 1 = V_{GS}^2 - 2V_{GS} + 1$$

$$V_{GS} = 2 \Rightarrow V_{o_{min}} = V_{GS} - V_t = 2 - 1 = 1V$$

$$V_R = 5 - 2 = 3 \Rightarrow R = \frac{3}{100 \mu A} = 30k\Omega$$

$$V_A = 10L = 10(10) = 100V \Rightarrow r_o = \frac{V_A}{I_o} = \frac{100}{100 \mu A} = 1M\Omega$$
Example 22

Want all transistors to operate in SAT

From above:

\[
\begin{align*}
I_2 &= \frac{(W/L)_2}{I_{REF}} \\
I_3 &= \frac{(W/L)_3}{I_{REF}} \\
I_5 &= \frac{(W/L)_5}{I_{REF}}
\end{align*}
\]

The threshold between saturation and linear region is: \( V_{DS}=(V_{GS}-V_t) \)

For Q2: \( V_{DS2}=V_{D2}-V_{S2}=0.5 \)
\( V_{GS2}=V_{D2}+V_{m}=1.5 \)

\[
I_2 = 50 \mu A = \frac{1}{2} k_n \left( \frac{W}{L} \right) (V_{GS1}-V_m)^2 = \frac{1}{2} \left( \frac{W}{L} \right) (1.5-1)^2
\]

\( W_2=200 \mu A \)

For Q5: \( V_{DS5}=V_{D5}-V_{S5}=-0.5 \)
\( V_{GS5}=V_{D5}+V_{m}=1.5 \)

\[
I_5 = 50 \mu A = \frac{1}{2} k_p \left( \frac{W}{L} \right) (V_{GS5}-V_m)^2 = \frac{1}{2} \left( \frac{W}{L} \right) (-1.5+1)^2
\]

\( W_5=500 \mu A \)

\[
I_2 = \frac{(W/L)_2}{I_{REF}} \quad \text{and} \quad I_5 = \frac{(W/L)_5}{I_{REF}} \Rightarrow W_1=40 \mu A \quad \text{and} \quad W_3=10 \mu A
\]

MOSFET Configurations

- **Common Source (CS)**
  -- best for high gain (most common)
  -- high input R
  - Puts source to gnd for AC analysis

- **Common-Drain (CD)**
  -- used for unity-gain voltage amplifier

- **Common Gate (CG)**
  -- low input R (bad for voltage gain, good to not attenuate current signal)
  -- used for unity-gain current amplifier
Example 22:

Capacitors frequency dependence \( \Rightarrow \frac{1}{C_j\omega} \)

DC Analysis \( \Rightarrow \) Open Caps and Find \( I_D \) (\( \omega=0 \) for DC signal so \( \frac{1}{\omega} = \infty \). It looks like a short)

\[
\begin{align*}
V_G &= \frac{10(5\mu)}{15\mu} = 3.38V \\
I_D &= \frac{1}{2}(2m)(3.33-I_D(3k)-1)^2 \\
I_D &= (1k) = (2.33-I_D(3k))^2 = 5.44 + I_D^2(3k)^2 - 13980I_D \\
I_D &= \frac{14980\pm\sqrt{(14980)^2 - 4(5.44)(3k)^2}}{2(3k)^2} = \frac{14980\pm5378}{18\mu} \\
I_D &= 1.1m, [+533\mu]
\end{align*}
\]

\( I_2 = 1.1m \Rightarrow V_S = 3.3V \)
\( \therefore V_{SS} = 0.03V < V_t \quad \text{NO} \)

\( I_D = 533\mu \Rightarrow V_S = 1.599, V_S = 1.731 > V_t \)
\( \therefore \text{ON} \)

\( V_D = 10 - 5k(533\mu) = 7.335 \)
\( \therefore V_D > V_G - V_t \) (SATV)

AC Analysis \( \Rightarrow \) Short Caps (\( C=\text{large so} \ \frac{1}{\infty} \to 0 \})

\[
\begin{align*}
g_m &= \sqrt{2K_n \left( \frac{W}{L} \right)}I_D = 1.5m = \sqrt{2*2e - 3*533e - 6} \\
V_o &= -g_m v_{gs} (5k \| 10k) \\
v_{gs} &= \frac{v_{sig}(3.33\mu)}{3.33\mu + 100k} \\
\frac{V_o}{v_{sig}} &= -4.85 \frac{V}{V}
\end{align*}
\]
Example 23: AC Analysis

This makes this amplifier a common-drain (CD) amplifier.

DC Analysis ⇒

\[
V_t = 1V, \quad K_n \left( \frac{W}{L} \right) = 6m, \quad \lambda = 0
\]

\[
V_o = I_D(10k) - 12
\]

\[
V_G = +12(6k) \quad \frac{12k + bk}{2} = 4V
\]

\[
I_D = \frac{1}{2} (6m)(4 - I_D(10k) + 12 - 1)^2
\]

\[
I_D = \frac{1.4m}{1.6m} \Rightarrow I_D = 1.6m
\]

\[
V_S = 2V \quad V_S = 4 \Rightarrow V_{GS} = 0V < V_t \quad \text{NO}
\]

\[
V_{GS} = 2V > V_t
\]

\[
V_D = +12V \quad (\text{SAT} \Rightarrow V_{DS} \geq V_{GS} - V_t)
\]

\[
\frac{V_o}{V_{sig}} = \frac{g_m V_{gs}(10k)}{1 + g_m(10k)} = 0.98 \frac{V}{V}
\]

Note: (Model T)

\[
R_{out} = \frac{1V}{I_t} \quad V_{gs} = -1V
\]

\[
I_t + g_m V_{gs} - I_t = 0 \Rightarrow I_t = g_m + \frac{1}{10k}
\]

\[
R_{out} = \frac{1V}{g_m + \frac{1}{10k}} = \frac{1}{g_m} \| 10k = 238\Omega
\]

\[
V_o = g_m V_{gs}(10k)
\]

\[
v_{gs} = V_{sig} - g_m V_{gs}(10k)
\]

\[
g_m = \sqrt{2(6m)1.4m} = 4.1m
\]

\[
\frac{V_o}{V_{sig}} = \frac{41}{1 + g_m(10k)} = 0.98 \frac{V}{V}
\]

\[
R_{out} = \frac{1V}{g_m + \frac{1}{10k}} = \frac{1}{g_m} \| 10k = 238\Omega
\]
Example 24:

**AC Analysis:**

\[ V_t = 1V, \quad K_n \left( \frac{W}{L} \right) = \frac{2mA}{V^2}, \quad \lambda = 0\]

\[ I_D = \frac{1}{2} (2m) (0 - I_D (7k) + 9 - 1)^2 \]

\[ I_D = \frac{1m}{2}, \quad 1.3m \Rightarrow I_D = 1.3m, \quad V_s = .1, \quad V_s = -0.1 < V_t \quad \text{NO} \]

\[ V_s = -2 \]

\[ V_{GS} = +2V > V_t \quad \text{(ON)} \]

\[ V_D = 9 - 5 = 4V \quad \text{(SAT)} \]

**DC Analysis:**

\[ +9V \]

\[ -9V \]

\[ V_G = 0 \]

\[ I_D \]

\[ -9V \]

\[ \frac{2mA}{V} \]

\[ V_0 = -g_m V_{gs} (5k \parallel 2k), \quad V_{gs} = -V_{sig} \]

\[ R_{in} = 7k \quad \frac{1}{g_m} = 467\Omega \]

\[ R_{out} = 5k \]
Common Source biased with current mirror:

$$\text{Gain} = \frac{V_D}{V_{input}} = g_m \cdot r_{o1}$$

Good gain => 20 to 100

Lousy $$r_o$$ (high)

Common drain (source follower) biased with current mirror:

$$v_o = g_{ms} \cdot r_o \cdot V_s$$

$$R'_S = \frac{1}{g_m + \frac{1}{r_{o2}} + \frac{1}{r_{o1}}}$$

$$\frac{v_o}{v_{in}} = \frac{g_m \cdot R'_S}{1 + g_m \cdot R'_S} = \frac{g_m}{g_m + \frac{1}{R'_S} + \frac{1}{R_L}}$$

$$R_o = \frac{1}{g_m + g_{mb} + \frac{1}{r_{o2}} + \frac{1}{r_{o1}}}$$

often neglected
Example 28

$V_i = 2V$

$k_n'(W/L) = 4mA/V^2$

Find $I_1$, $I_D$, $I_S$, $I_L$

Find $V_G$, $V_S$, $V_o$

Find $R_{in}$, $A_v = V_o / V_i$

Dr. Rasmussen    Spring 2011
Frequency Response:

- The low frequency is typically determined by the coupling capacitors.
  - These are controlled by the designer.

**EX:**

\[ V_{o} = -g_{m}R_{D} \]

\[ V_{gs} = V_{i} - g_{m}V_{gs}(R_{s}||C_{s}) \]

\[ V_{o} = \frac{-g_{m}R_{D}(R_{s}C_{s}+1)}{(1+g_{m}R_{s})(R_{s}C_{s}+1)} \]

- Leave capacitors in the AC model to determine overall transfer function →
\[
\frac{V_o}{V_i} = -g_m \frac{R_D}{(1+g_m R_s)} \left[ \frac{R_s C_1 s + 1}{(R_s C_1 s + 1) + 1} \right]
\]

Magnitude plot \(\Rightarrow\)  
One zero @ \((R_s C_1 s + 1) = 0\)  
\[ S = \frac{1}{R_s C_1} \]

One pole at \((\frac{R_s C_1}{1+g_m R_s} + 1) = 0\)  
\[ S = \frac{R_s C_1}{1+g_m R_s} \]

\[ \text{The pole will be larger than the zero} \]

Recall that a zero contributes \(+20\,\text{dB/dec}\) and a pole \(-20\,\text{dB/dec}\).

Suppose you want the low freq. to be 10 Hz  
\[ 10 \,\text{Hz} = \frac{(1+g_m R_s)}{2\pi (R_s C_1)} \Rightarrow C_1 \approx 18.6 \,\mu\text{F} \]  
(when \(g_m = 1\,\text{m}, R_s = 6\,\text{k}\))
High Frequency: Controlled by parasitic capacitance

\[ I_L = g_m V_{gs} - I_{gd} \quad \text{(at frequencies } \approx f_T \text{ assume } I_{gd} < g_m V_{gs}) \]

\[ V_o \approx -g_m R'_L V_{gs} \]

\[ I_{gd} = \frac{V_g - V_o}{C_{gd}} (V_{gs} - (-g_m R'_L V_{gs})) \]

\[ I_{gd} = C_{gd} \cdot \frac{V_o}{R_o + R_{sig}} \]

Since \( I_{gd} \) does not influence the output, it can be modified:

where

\[ V_o = \frac{V_{gs} - \frac{I_{gd}}{g_m V_{gs}}}{R_{o + R_{sig}}} \]

\[ R_{sig}' = R_{sig} || R_L \]

Thevenin equivalent
From new circuit,

\[ I_{gd} = \frac{V_{gs}}{C_{eq} \cdot S} = C_{eq} \cdot S \cdot V_{gs} \]

Setting old \( I_{gd} = \) new \( I_{gd} \)

\[ C_{eq} \cdot S \cdot V_{gs} = C_{gd} \cdot S \cdot \left( 1 + g_m R'_L \right) V_{gs} \]

\[ C_{eq} = C_{gd} \left( 1 + g_m R'_L \right) \]

\[ V_{gs} = \frac{V_{sig} \left( R_g \right)}{R_G + R_{sig}} \left( \frac{1}{C_{gs} \cdot S} + \frac{1}{S \left( C_{eq} + C_{gs} \right)} \right) \]

\[ \frac{1}{C_{gs} \cdot S} \parallel \frac{1}{C_{eq} \cdot S} = \frac{1}{S \left( C_{eq} + C_{gs} \right)} \]

\[ V_{gs} = \frac{V_{sig} \cdot R_G}{\left( R_G + R_{sig} \right) S \left( C_{eq} + C_{gs} \right)} \]

Recall \( V_0 = -g_m R'_L V_{gs} \Rightarrow \)

\[ V_0 = \frac{-g_m R'_L R_G}{R_G + R_{sig}} \left( 1 + S R_{sig} \left( C_{eq} + C_{gs} \right) \right) \]

With only 1 pole \Rightarrow \] (recall \( -20 \text{dB/dec} \))

\[ W_H = \frac{1}{R_{sig} \left( C_{eq} + C_{gs} \right)} \]
Example:

\[
g_m = 1 \text{mA/V}
\]

\[
C_{gs} = 1 \text{pF}
\]

\[
C_{gd} = 0.2 \text{pF}
\]

Let us analyze low freq. 1st ⇒

\[C_g, C_s, \text{ and } C_r \text{ contribute to low response (ignore parasitics } C_{gs}, C_{gd})\]

\[
V_o = \left[\frac{-g_m V_{gs} \cdot 4.7K}{4.7K + \frac{1}{C_s} + 10K}\right] \cdot 10K = \frac{-g_m 4.7K (10K) V_{gs} \cdot C_s}{(14.7K) C_s + 1}
\]

\[
V_{gs} = \frac{V_{sig} (8.25M)}{8.25M + 100K + \frac{1}{C_s}} - g_m V_{gs} \cdot \frac{2k\|}{C_s}
\]

\[
V_{gs} = \frac{V_{sig} (8.25M) C_s}{(8.35M C_g \cdot C_s + 1)} - \frac{1}{1 + g_m (2k\| C_s)}
\]
\[ V_{gs} = \frac{V_{sig} (8.25M)C_{a}.S (2K.C_{s}.S +1)}{(8.35M.C_{a}.S+1)(1+g_{m}2K)(\frac{2K.C_{s}.S +1}{1+g_{m}2K})} \]

\[ \frac{V_{o}}{V_{sig}} = \frac{-4.7m(0.0825)(0.02s+1).S^{2}}{(1.47m.S+1)(0.0835.S+1)(3)(6.67m.S+1)} \]

poles at \( w = 680.3 \text{ rad/sec} \rightarrow (R_o+R_i)C_L \)
\( w = 12 \text{ rad/sec} \rightarrow \frac{1}{(R_o+R_{sig}).C_G} \)
\( w = 150 \text{ rad/sec} \rightarrow \frac{1}{(g_{m}/R_s).C_s} \)

zero at \( w = 500 \text{ rad/sec} \)

This circuit will start to work properly at \( f_L = 108 \text{ Hz} \).

High frequency \( \Rightarrow \) (Recall derivation)

\[ w_H = R_{sig}(C_{eq}+C_{gs}) \]
where \( R_{sig} = 100K/18.25M \)
\( R_{sig} = 98.802K \)

\( C_{eq} \Rightarrow \) (Short all external caps and only look at \( C_{gs} \) and \( C_{gd} \))

\[ C_{eq} = C_{gd} (1+g_{m}(4.7K/110K)) = 0.84 \text{ pF} \]

\[ w_H = \frac{1}{98.802K(0.84+1)p} = 5.5 \text{ rad/sec} \]

\[ f_H \approx 8.76 \text{ Hz} \]
Introduction to Bipolar Junction Transistors (BJTs)

A transistor has three terminals—the base, the collector, and the emitter. The current flow from the collector to the emitter (through the transistor) is controlled by the current flow from the base to the emitter. A small base current can control a much larger collector current.

Bipolar junction transistors (BJTs) consist of three layers of doped silicon. The NPN transistor has a thin layer of P-doped silicon sandwiched between two layers of N-doped silicon. Each P-N junction can act like a diode. In fact, this is a fairly good way to check a transistor with an ohmmeter (set to the diode setting).

The base-emitter junction always acts like a diode, but because the base is very thin, it makes the other junction act like a controlled valve (details to come later).

Very High Level Overview of how a transistor works:

- A small amount of base current controls a large emitter (collector) current

Analogy:
- Think of the transistor as an “electronic” tap able to control a large flow of electrons (from collector to emitter) with only a small variation in the “handle” (base)
- Water Tap Analogy: (water spigot)
  → Large amounts of H₂O controlled by very small movement of the tap

BJT Operation

Modes or regions of operation

<table>
<thead>
<tr>
<th>Cutoff (off)</th>
<th>Active (partially on)</th>
<th>Saturation (fully on)</th>
</tr>
</thead>
<tbody>
<tr>
<td>v_BE &lt; 0.7 V</td>
<td>v_BE &gt; 0.7 V, i_B &gt; 0</td>
<td>v_CE = 0.2 to 0.7 V, i_C &lt; βi_B</td>
</tr>
<tr>
<td>i_B = 0, i_C = 0</td>
<td>v_CE ≥ 0.7 V, i_C = βi_B</td>
<td>i_C = βi_B limited by something outside of the transistor</td>
</tr>
</tbody>
</table>

Typical transistor curves

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Summary of BJT Current-Voltage Relationships in the Active Mode:

\[ i_C = I_S e^{v_{BE}/V_T} \]  \( n=1 \) always for BJT \{Ebers-Moll equation\}

\[ i_B = \frac{i_C}{\beta} = \left( \frac{I_S}{\beta} \right) e^{v_{BE}/V_T} \]

\[ i_E = \frac{i_C}{\alpha} = \left( \frac{I_S}{\alpha} \right) e^{v_{BE}/V_T} \]

Note: For the pnp transistor, replace \( v_{BE} \) with \( v_{EB} \)

\[ I_C = \alpha I_E = \beta I_B \quad I_E = (\beta+1)I_B \quad \beta = \frac{\alpha}{1-\alpha} \quad \alpha = \frac{\beta}{\beta+1} \]

\( V_T \) = thermal voltage \( \cong \) 25mV at room temperature

Temperature dependencies
\[ v_{BE} = 0.7V \] (decreases about 2.1 mV / °C)

at constant \( I_C \):
\[ \Delta v_{BE} = -2.1\text{mV/}^\circ\text{C} \]

at constant \( V_{BE} \): \( I_C \) increases by 8% per °C (10x per 30°C)

Method for solving DC voltages and currents of a BJT circuit:

1). Start by assuming transistor is in active mode
   Either use given values for base-emitter voltage, or use
   \[ V_{BE} = 0.7V \] (nnp)
   \[ V_{EB} = 0.7V \] (pnp)

2). Solve for the BJT node voltages and currents
   - Voltages: sometimes can read off directly, otherwise use loop equation
   - Once you have one current, you can get the other two from the active mode equations

3). Check to see if the solution is consistent!
   \[ V_C \geq V_B > V_E \]  \( \text{nnp active} \) more explicitly: \( V_{CB} \geq 0, V_{BE} \geq 0.7V \)
   \[ V_E \geq V_B \geq V_C \]  \( \text{pnp active} \) more explicitly: \( V_{CB} \geq 0, V_{EB} \geq 0.7V \)

4). If the solution is consistent, stop \( \Rightarrow \) you are done
   If not, the transistor is either in saturation or cutoff
   \( \Rightarrow \) go to 2), however active mode equations \textbf{do not} apply!
   \( \Rightarrow \) Now use: saturation: \( v_{BE} \approx 0.7V \) and \( v_{CE} \approx 0.2V \) for nnp
   \( v_{EB} \approx 0.7V \) and \( v_{EC} \approx 0.2V \) for pnp
   cutoff: set all currents to approximately 0:
   \[ i_C = 0 \quad i_E = 0 \quad i_B = 0 \]

\textbf{NPN ACTIVE AND ON when:}
\[ v_{BE} \geq V_{Beon} \quad (V_{Beon} \cong 0.5V) \]
\[ V_C \geq V_B > V_E \] and \( V_{CE} > 0.2V \)

\textbf{PNP ACTIVE AND ON when:}
\[ v_{EB} \geq V_{Ebon} \]
\[ V_E \geq V_B \geq V_C \] and \( V_{EC} > 0.2V \)
Example 29:
Find $V_E$ and $I_C$ for each circuit. Assume that $|V_{BE}| = 0.7\text{V}$ and $\beta = 40$. Both transistors are being operated in the active mode.

(a) NPN

\[
\begin{align*}
V_E &= 5 - 0.7 = 4.3\text{V} \\
I_E &= \frac{V_E}{R_E} = \frac{4.3}{1k} = 4.3\text{mA} \\
I_c &= \frac{\beta}{\beta + 1} I_E = \frac{40}{41}(4.3\text{mA}) = 4.2\text{mA}
\end{align*}
\]

Check:
$V_C = 7.8\text{V} \geq V_B = 5\text{V} > V_E = 4.3\text{V}$

(b) PNP

\[
\begin{align*}
V_E &= 0.7\text{V} \\
I_E &= \frac{10 - 0.7}{2k} \approx 4.7\text{mA} \\
I_c &= \frac{\beta}{\beta + 1} I_E = 4.5\text{mA}
\end{align*}
\]

Check:
$V_E = 0.7\text{V} > V_B = 0 \geq V_C = -5.5\text{V}$

Example 30:

Given: $|V_{BE}| = 0.7\text{V}$

Find: $I_C$, $V_C$, and $V_E$

Recall: For active mode pnp, should have $V_E > V_B > V_C$

(All dc, so use caps)

1). Assume active mode
2). Solve:
\[
\begin{align*}
V_E &= V_B + 0.7\text{V} = 1.7\text{V} (V_B = 1\text{V}) \\
I_E &= \frac{6 - V_E}{10k} = \frac{6 - 1.7}{10k} = 0.43\text{mA} \\
I_c &= \frac{\beta}{\beta + 1} I_E \approx 0.43\text{mA} \\
V_C &= 10k(I_c) = 4.3\text{V}
\end{align*}
\]

3). Check: $V_C = 4.3 > V_B = 1\text{V}$ → cannot be active
4). Start over with assumption that transistor is cutoff:
   To see if cutoff, set all currents to 0 or in other words take transistor out of circuit and should get $V_B > V_E$ and $V_B > V_C$

\[
\begin{align*}
V_E &= 6\text{V}, \ V_B = 1\text{V} \rightarrow V_E > V_B \rightarrow \text{Can not be cutoff (pnp!!)}
\end{align*}
\]

Transistor must be saturated:
To see if saturation, set $V_{EB} = 0.7\text{V}$ and $V_{EC} = 0.2\text{V}$
And should get $V_C > V_B$ for FB CBJ

Need to recalculate values (i.e. ones from active mode assumption are not valid)
Active mode equations do not apply → need to just use $V=IR$, KVL, KCL

Saturation analysis=>
\[
\begin{align*}
V_E &= V_B + 0.7 = 1.7 \\
I_E &= 0.43\text{mA} \\
V_C &= 1.7 - 0.2 = 1.5\text{V} \\
I_C &= \frac{1.5}{10k} = 0.15\text{mA} \\
V_{CB} &= 0.7 - 0.2 = 0.5\text{V} \\
V_C > V_B \rightarrow \text{It is saturated!}
\end{align*}
\]

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Example 31

\[ \beta = 100 \]

\[ V_{BB} = I_B R_{BB} + V_{BE} + I_E R_E \]

\[ I_B = \frac{I_E}{\beta + 1} \]

\[ I_E = \frac{V_{BB} - V_{BE}}{R_E + \left( \frac{R_{BB}}{(\beta + 1)} \right) \frac{33.3k}{101}} = 1.29mA \]

\[ V_E = I_E R_E = (1.29mA)(3k) = 3.87V \]

\[ I_B = \frac{1.29mA}{101} = 12.8mA \]

\[ V_B = V_{BE} + V_E = 0.7 + 3.87 = 4.57V \]

\[ I_C = \alpha d_E = 0.99(1.29m) = 1.28mA \]

\[ V_C = 15V - I_C R_C = 15V - (1.28m)(5k) = 8.6V \]

**Temperature Effects:**

NPN Transistor Characteristic

\[ T_3 > T_2 > T_1 \]

As \( T \uparrow, I \uparrow \) for fixed \( V_{BE} \)

**Early Voltage and output resistance**

\( \beta \) depends on the effective base width, \( W \) which depends on \( V_{CB} \). This leads to the Early effect, which is expressed as an output resistance.

\[ \text{Early voltage.} \]

\[ \text{Output resistance} = r_o = \frac{V_A}{I_C} \]

Thevenin:

\( R_{BB} = 100k\Omega \| 50k = 33.3k \)

Voltage divider for \( V_{BB} = 5V \)

**Thermal runaway:**

\( T \uparrow \rightarrow I_C \uparrow \rightarrow P_D \uparrow \rightarrow T \uparrow \rightarrow I_C \uparrow \rightarrow P_D \uparrow \rightarrow \ldots \)
Bipolar Junction Transistor (BJT) bias in the active region

Bias: Want a stable \( I_C \) for any transistor at any temperature
To work as an linear amplifier, a transistor must operate in the active region. To work in the active region \( I_B \) and \( I_C \) must be positive for all values of the AC signals — they must be biased to some positive DC value. The AC signals will swing above and below these DC values. Furthermore, the transistor must not saturate, or it will lose control of \( I_C \).

Bias should not depend too much on the value of \( \beta \)
\( \beta \) can vary widely from transistor to transistor of the same part number. No one wants to individually test transistors to find ones that will work in your circuit.

Bias should not depend too much on the value of \( V_{BB} \)
The relationship between \( V_{BB} \) and \( I_C \) is far too dependent on temperature and, like \( \beta \), varies from transistor to transistor.

Stable bias set by a stable \( V_R \) and an \( R_E \)
As we saw last time if we set \( V_B \) with a battery \( (V_{BB}) \) then \( I_C \) is very stable. Instead of \( I_B \) controlling \( I_C \) through the unpredictable \( \beta \), a stable \( V_B \) sets \( V_E \) \((V_B - 0.7V)\) and \( R_E \) sets \( I_E \) and hence \( I_C \). \( I_B \) then takes care of itself, and adjusts to compensate for different \( \beta \)s and temperatures. Unfortunately it's pretty impractical. You don't want two power supplies and besides, you can't get a signal to the base. Still, most schemes to achieve stable bias work by setting a stable voltage at the base for any reasonable \( I_B \).

Voltage-divider bias
To make the left circuit look like the right one:

\[
V_{BB} = \frac{R_B}{R_{B1} + R_{B2}} \quad V_{CC} = \frac{R_B}{R_{B1} + R_{B2}} \quad R_{BB} = \frac{1}{\frac{1}{R_{B1}} + \frac{1}{R_{B2}}}
\]

Both circuits:

\[
I_B = \frac{V_{BB} - 0.7V}{R_{BB} + (\beta + 1)R_E}
\]

\[
I_C = \beta I_B \simeq I_E
\]

Use Thevenin's analysis
Note: Often in quick-and-dirty analysis you can neglect the base current, \( I_B \). In that case:

\[
V_B = V_{BB} \quad V_E = V_B - 0.7V \quad I_E = \frac{V_E}{R_E} \simeq I_C
\]

This assumption is \( \beta \): \( R_{BB} < \beta R_E \)
Quick check: \( R_{B1} < 10 \times R_E \) OR \( R_{B2} < 10 \times R_E \) Should result in \(<1\% \) error if \( \beta \geq 100 \)

\[
V_C = V_{CC} - I_C R_C \quad V_E = I_E R_E
\]

Always check that \( V_{CE} > 0.2V \) to see if the circuit was really in the active region.

What if \( V_{EE} \) is not ground?

\[
V_{BB} = (V_{CC} - V_{EE}) \frac{R_B}{R_{B1} + R_{B2}} + V_{EE} \quad R_{BB} = \frac{1}{\frac{1}{R_{B1}} + \frac{1}{R_{B2}}}
\]

\[
I_B = \frac{V_{BB} - 0.7V - V_{EE}}{R_{BB} + (\beta + 1)R_E}
\]

\[
I_C = \beta I_B \simeq I_E
\]

If you can neglect the base current, \( I_B \). In that case:

\[
V_B = V_{BB} \quad V_E = V_B - 0.7V \quad I_E = \frac{V_E - V_{EE}}{R_E} \simeq I_C
\]

\[
V_C = V_{CC} - I_C R_C \quad V_E = I_E R_E + V_{EE} \quad V_{CE} = V_C - V_E \quad \text{Always check that \( V_{CE} > 0.2V \) to see if the circuit was really in the active region.}
\]

The equations above and on the last page are for the circuits shown, adapt them as necessary to fit your actual circuit.
BJT Bias Design

Decisions that you make for the bias will affect many other qualities of the circuit, so you should know some of your wants and expectations up front. See the tradeoffs below. Design is often an iterative process. Try something, see if it works, modify, try again. The parameters below are listed in good order for design, i.e. you usually start by selecting $I_C$.

**select**
- $I_C$
- lower value: less power from supply
- lower power dissipated in transistor
- higher input impedance

**Tradeoffs**
- higher value: larger available output voltage swing
- more output power available
- lower output impedance

Don't want $\beta$ variations to affect $I_C$, so make sure that $I_B$ is the one to vary when $\beta$ changes: Usually make $\beta R_E > R_{BB}$.

Temperature effects on $I_C$:
$$\frac{\Delta V_{BE}}{\Delta T} = 2.1 \text{ mV/degC (constant } I_C \text{)}$$

For every 60 mV increase in $V_{BE}$, $I_C$ will increase by factor of 10.

If $V_{BE}$ is held constant, $I_C$ will increase by factor of 10 for every 30 °C increase in temperature.

Try to swamp the $V_{BE}$ changes with a much bigger voltage across $R_E$. For a temperature range of

Ex: 0 to 40 °C, $V_{BE}$ changes 84 mV.

$$24 \cdot 84 \text{ mV} = 2 \cdot V \quad V_E = 2 \text{ V swamps } \Delta V_{BE} \text{ pretty well (24x).}$$

**select**
- $V_E$
- (CE & CB amps) larger available output voltage swing
- (CC amp) Bias for output swing requirements

**Tradeoffs**
- higher value: Better $\beta$ and thermal stability
- (CC & CB, CE if unbypassed) higher input impedance

$$R_E = \frac{V_E}{I_C}$$

$V_B = V_E + 0.7 \text{ V}$

This will dictate ratio of

$$\frac{R_{B2}}{R_{B1}} = \frac{V_{BB} - V_{EE}}{V_{CC} - V_{BB}}$$

**select**
- $R_{B1}$ & $R_{B2}$
- Better $\beta$ stability

**Tradeoffs**
- (CE & CC) higher input impedance
- less power from supply

A couple of other bias schemes

![Diagrams of various bias schemes]

Taken to extremes, $I_C$ is now very stable at:

$$I_C = \frac{V_{CC} - 0.7 \cdot V}{R_C}$$

Seems like a useless circuit, but...
Current source bias: We could make the bias current very stable if we had a current source.

If we can make current sources (drains), then...

For a perfect current source, \( R_E = \infty \)

Current mirrors: A way to make a current source (drain)

\[
I_C = \frac{V_{CC} - V_{EE} - 0.7V}{R_C} = I_{ref}
\]

Recall that \( V_{BE} \) is really not exactly 0.7V, from Ebers-Moll eq.: \( I_C = I_S e^{\frac{V_{BE}}{V_T}} \)

Because \( V_{BE1} = V_{BE2} \), \( I_C = I_{C2} \)

We can get a current source (usually called a current drain in this type of configuration). I could make a positive source if I used PNP transistors.

But, the transistors must be identical, and at the same temperature, like in an IC.

Example:

Say: \( V_{CC} = 7\) V

\( R_E \) is very common in transistor circuits. If the collector current is fluctuating according to some signal, those fluctuations will cause voltage fluctuations across \( R_E \), which could be the output signal voltage of the circuit.

What if we want \( I_C = 10\) mA and \( V_C = 3\) V

Then \( R_C = V_{CC} - V_C \)

\( R_C = 400\) Ω

Let's assume that \( \beta = 200 \)

\[
I_B = \frac{I_C}{\beta} \quad I_B = 0.05\text{mA}
\]

Say \( V_{BB} = 2.5\) V

Then \( R_{BB} = \frac{V_{BB} - 0.7V}{I_B} \)

\( R_{BB} = 36\) kΩ

All looks hunky-dory, right?

What if \( \beta = 100 \)?

\[
I_B = \frac{V_{BB} - 0.7V}{R_{BB}} = 0.05\text{mA}
\]

no change here, looks good so far.

\[
I_C = \beta I_B \quad I_C = 5\text{mA}
\]

Yuk, that changed by half.

\[
V_C = V_{CC} - I_C R_C \quad V_C = 5\text{V}
\]

At least \( V_C \) only changed by 2V. Still, that may be too much.

At least we're still in the active region (\( V_{CE} > 0.2\) V).

What if \( \beta = 400 \)?

\[
\begin{align*}
I_B &= \frac{V_{BB} - 0.7V}{R_{BB}} = 0.05\text{mA} \\
I_C &= \beta I_B &= 20\text{mA} \\
V_C &= V_{CC} - I_C R_C &= -1\text{V}
\end{align*}
\]

Oops, that can't be good. In fact, we have to assume that we're out of the active region -- way bad...

Must recalculate \( I_C \) and \( V_C \):

\( V_C = 0.2\) V (Saturation)

\[
I_C = \frac{V_{CC} - 0.2V}{R_C} = 17\text{mA}
\]

Let's try a little different approach:

Again, let's design for \( I_C = 10\) mA

\[
V_E = V_{BB} - 0.7V
\]

It is common here to assume:

\[
I_E = I_C
\]

but actually,

\[
I_C = \alpha I_E = \frac{\beta + 1}{\beta + 1} I_E
\]

if \( \beta = 100 \)

\[
\alpha = \frac{\beta}{\beta + 1} \quad I_C = \alpha I_E = 9.901\text{mA} \quad I_B = \frac{I_C}{\beta} = 0.1\text{mA}
\]

if \( \beta = 400 \)

\[
I_C = \frac{\beta}{\beta + 1} I_E = 9.975\text{mA} \quad I_B = \frac{I_C}{\beta} = 0.025\text{mA}
\]

Now that's more like it, now \( I_B \) changes instead of \( I_C \).
BJT basic amplifier:

DC:

\[ I_C = I_s e^{v_{BE}/V_T} \]
\[ I_E = \frac{I_C}{\alpha} \]
\[ I_B = \frac{I_C}{\beta} \]
\[ V_C = V_{CE} = V_{CC} - I_C R_C \]

Look at signal component only:

\[ i_c = \frac{I_C}{V_T} v_{be} \]

Transconductance

Dynamic forward resistance of BE junction

Input Resistance:

\[ r_c = \frac{V}{i_c} \]

Summary of ac parameters:

\[ g_m = \frac{I_C}{V_T} \]
\[ r_\pi = \frac{V_T}{I_B} = \frac{\beta}{g_m} \]
\[ r_o = \frac{V_A}{I_c} \]
\[ r_e = \frac{V_T}{I_E} \]

\[ i_c = g_m v_{be} \]
\[ V_c = -g_m R_c \]
Small-signal equivalent circuit models

Same concept as that of the MOSFET.

Small-signal equivalent circuit models

\[ r_π = (β + 1) r_c \]

\[ i_b = \frac{v_π}{r_π} \]

\[ β \cdot i_b = β \cdot \frac{v_π}{r_π} = β \cdot \frac{v_π}{(β + 1) r_c} \]

\[ g_m = \frac{β}{(β + 1) r_c} = \frac{α}{r_e} \approx \frac{1}{r_e} \]

Method for analyzing transistor amplifier circuits:

1. Determine dc operating point, specifically \( I_C \)
   (Set ac sources to 0!!)
   Note: Use method for analyzing BJT circuits at DC
2. Calculate small-signal parameters: \( g_m \), \( r_π \), and/or \( r_e \)
3. Set dc sources to 0
4. Replace the transistor with one of the equivalent small-signal models
5. Analyze the circuit as usual \( \rightarrow \) linear circuit analysis

Example

Circuit:
\( β = 100 \), \( V_{BB} = 3V \), \( R_C = 3k \)
\( R_B = 100k \), \( V_{CC} = 10V \)

Find the voltage gain, \( V_o/V_i \)

1. DC analysis: set \( v_i \) to 0
   Assume \( V_{BE} = 0.7V \)
   Assume active

Redraw circuit with just dc part:
\[ I_B = \frac{V_{BB} - V_{BE}}{R_{BB}} = \frac{3 - 0.7}{100} = 0.023mA \]
\[ I_C = β I_B = 2.3mA \]
\[ V_C = V_{CC} - I_C R_C = 10 - 2.3(3) = 3.1V \]
Double check your values:
\( V_C > V_B > V_E \ 3.1 > 0.7 > 0 \) YES!
2). Calculate small-signal parameters:

\[ g_m = \frac{I_C}{V_T} = \frac{2.3}{25} = 92\,mA/V \quad r_e = \frac{V_T}{I_E} = \frac{25}{(2.3/0.99)} = 10.8\,\Omega \quad r_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09\,k\Omega \]

3). And 4). Set dc sources to 0 and replace transistor with equivalent model.

Model:

5). Find requested gain: \( \frac{v_o}{v_i} = \frac{v_c}{v_i} \) We know \( v_o = v_c = -g_m v_{be} R_C \)

Now need \( v_{be} \) in terms of \( v_i \)

Voltage division:

\[ v_{be} = \frac{r_\pi}{r_\pi + 100k} v_i \]

\[ \frac{v_o}{v_i} = -g_m \frac{r_\pi}{r_\pi + 100k} R_C = -92.3k \frac{1.09k}{100k + 1.09k} = -3.04V/V \]

Resistance-Reflection Rule Between Base and Emitter:

via simultaneous equations:

\[ i_x = i_1 + i_2 \]

\[ i_1 = \frac{v_x}{R_E}, \quad i_2 = -i_e = -(i_b + i_c) = -i_b (\beta + 1) \]

\[ v_\pi = i_b r_\pi, \quad i_c = g_m v_\pi \]

etc.

\[ R_x = R_E \parallel \frac{r_\pi + R_B}{(\beta+1)} \parallel (r_o + R_e) \approx R_E \parallel (r_e + \frac{R_B}{(\beta+1)}) \]

a simple resistive network remains
Same problem, but look into base instead: \( R = ? \)

\[
R = R_B \| (r^\pi + (\beta+1)(R_E \| (r_o + R_c)))
\]

**Summary of Resistance-Reflection Rule between base and emitter:**
- Applies only when you want to reflect a resistor from emitter to base or base to emitter circuit

**Review of rule:**
1. Temporarily remove dependent source \( \beta \bar{i}_b \) or \( g_m v_{b\pi} \)
2. When looking into base: Replace resistors on emitter side with \( "R" \times (\beta + 1) \) or when looking into emitter: Replace resistors on base side with \( "R" \div (\beta + 1) \)
3. Treat circuit as a resistive network and find equivalent resistance

**This works because** \( i_b = \frac{i_e}{\beta + 1} \)

**In a nutshell:** To reflect a resistor from:
- \( E \rightarrow B \) multiply by \( \beta + 1 \)
- \( B \rightarrow E \) divide by \( \beta + 1 \)

**Things to keep in mind:**
- Rule does NOT work for impedance looking into collector – it is a reflection rule between base and emitter
- It works because \( i_b = \frac{i_e}{\beta + 1} \) which is a relationship between the base and emitter current!
- Finding \( R_{in} \) or \( R_{out} \) – this is just finding Thevenin equivalent resistance, \( R_{Th} \)
- Possible methods now that you can use:
  1. Using the resistance Reflection Rule
  2. Using Thevenin equivalent methods—use these to double check homework, but on exam will not likely have time
- \( R_{in} \) or \( R_{out} \) is always between a node and ground – follow all paths to ground from that node
- Applying the Reflection Rule is like turning off dependent sources and multiplying resistances by \( (\beta + 1) \) or dividing resistance by \( (\beta + 1) \) and treating circuit as just a resistive network – Note that this only works because the dependent source is being accounted for through the \( (\beta + 1) \) factor!

**Example:** Assume the transistors below have a finite \( \beta \) and an infinite Early voltage.
- Write an expression for the input resistance \( R_{in} \) in the circuit shown below. Your expression should include only real resistances \( (R_1, R_2, R_3, \text{ or a subset of these}) \) and possibly \( \beta, r_{e1} \) or \( r_{e2} \), and \( r_{o1} \text{ or } r_{o2} \). (Assume both transistors have the same \( \beta \).) Circle your answer. Hint: Use Resistance-Reflection rule
Common-Base

\[ \frac{V_o}{V_{\text{sig}}} = g_{m2} \left( \frac{R_2}{R_L} \right) \left( R_4 \left| \frac{r_{\pi2}}{\beta + 1} \right| + R_3 \right) \left( R_{\text{in}} + R_{\text{sig}} \right) \]

\[ V_{\pi2} = -V_1 \left( \frac{R_4}{R_4} \left| \frac{r_{\pi2}}{\beta + 1} \right| + R_3 \right) \]

\[ V_i = \frac{V_{\text{sig}} (R_{\text{in}})}{R_{\text{in}} + R_{\text{sig}}} \]

\[ C_1 = 10 \text{ pF}, \quad C_2 = 10 \text{ nF}, \quad \beta = 100 \]

Ignore \( r_o \)

\[ R_{\text{out}} = R_2 \]

\[ R_{\text{in}} = \frac{r_{\pi1}}{\beta + 1} \left( \frac{R_3 + R_4}{\beta + 1} \right) \]

Low frequency poles ⇒

1. \[ \frac{1}{C_2 (R_2 + R_L)} \]
2. \[ \frac{1}{C_1 (R_{\text{sig}} + R_{\text{in}})} \]

Capacitor * (R seen at cap nodes)

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2 Stage ⇒ Common Collector/Common Base

\[
V_o = -g_{m2} V_{\pi 2} \left( R_2 \| R_L \right)
\]

\[
V_{\pi 2} = \frac{-V_1 \left( \frac{R_4}{R_1} \right) \left( \frac{r_{\pi 2}}{\beta + 1} \right) + R_3}{R_4 \left( \frac{r_{\pi 2}}{\beta + 1} \right) + R_1}
\]

\[
V_1 = \frac{V_{in} \cdot R_{eq 1}}{R_{eq 1} + r_{\pi 1}}
\]

\[
V_{in} = \frac{V_{sig} \cdot R_{in}}{R_{in} + R_{sig}}
\]

Low frequency poles ⇒

1. \( \frac{1}{C_2 (R_2 + R_L)} \)
2. \( \frac{1}{C_3 \cdot R_1} \)
3. \( \frac{1}{C_1 \left( R_{sig} + R_{in} \right)} \)
2 Stage ⇒ Common-Emitter/Common-Collector

Low frequency poles ⇒ NOTE THAT C₄ IS NOT SEEN BY OUTPUT – Do not need

\[ \frac{1}{C_1(R_{\text{sig}} + R_{\text{in}})} \quad \text{en} \quad \frac{1}{C_2 \cdot R_3} \quad \frac{1}{C_3 \left( R_1 + \frac{R_6}{\beta + 1} \right)} \quad \text{ing} \quad \frac{1}{C_4 \cdot R_2} \]
Common collector (CC)

The circuits shown are typical arrangements. Note that \( V_{EE} \) is often 0 V (ground). The equations below are for these circuits, adapt them as necessary to fit your actual circuit.

Voltage gain about 1. Good for current gain, or to match a high impedance source to a low impedance load.

The small-signal emitter resistance is right in the emitter of the transistor (where the arrow is).

Recall that the emitter resistor looks \( \beta \) times as big from the base's point-of-view. That's also true for signals

Input impedance:
\[
R_i = R_B || R_B || \beta \left( r_e + R_E || R_L \right)
\]

The opposite effect also works, resistors at the base look \( \beta \) times smaller from the emitter's point-of-view.

Output impedance:
\[
R_o = R_E || r_e + R_B || R_B || R_S \frac{1}{\beta}
\]

Low frequency corner frequencies

\[
f_{CL1} = \frac{1}{2 \pi \left( R_S + R_i \right) C_{in}} \quad f_{CL2} = \frac{1}{2 \pi \left( R_L + R_o \right) C_{out}}
\]

From the signal analysis, the only thing between the base signal and the output signal is \( r_e \). To find the output, just use the voltage divider equation.

Voltage gain:
\[
A_v = \frac{v_o}{v_b} = \frac{R_E || R_L}{r_e + R_E || R_L} \approx 1
\]

OR:
\[
A_v = \frac{v_o}{v_s} = \frac{R_i}{R_S + R_i} \frac{R_E || R_L}{r_e + R_E || R_L}
\]

You could think of the output as simply 0.7V DC less than the input, which doesn't make the AC signal any less. Of course this doesn't account for the \( r_e \) effects.

Current gain:
\[
A_i = \frac{i_o}{i_i} = \frac{R_E || R_L}{r_e + R_E || R_L} \frac{R_i}{R_L} = A_v \frac{R_i}{R_L} \approx \frac{R_i}{R_L}
\]

Common emitter (CE)

Now let's add a resistor in the collector (\( R_C \)). Nearly the same current that flows through \( R_E \) flows through \( R_C \).

\[
v_c = -i_c R_C \quad v_e = i_e R_E \quad v_b
\]

\[
i_c \approx i_e \quad \text{so:} \quad \frac{v_c}{v_b} \approx \frac{R_C}{R_E} \text{ gain}
\]
Common emitter (CE)

Common Emitter amplifier, example:

Bias:
\[ V_{BB} = \frac{R_{B2}}{R_{B2} + R_{B1}} V_{CC} \]
\[ V_{BB} = 1.782 \cdot V \]
\[ R_{BB} = 1.479 \cdot k\Omega \]

\[ I_B = \frac{V_{BB} - 0.7 \cdot V}{R_{BB} + \beta R_E} \]
\[ I_B = 0.056 \cdot mA \]
\[ I_E = \frac{V_E}{R_E} \]
\[ I_C = I_E \]
\[ I_C = 10 \cdot mA \]

What if we put in an AC input signal:
\[ i_C(t) : = \frac{v_E(t)}{R_E} \]
\[ V_C(t) : = V_{CC} - i_C(t) R_C \]
\[ V_B(t) : = V_B + 0.5 \cdot V \cdot \cos \left( \frac{6280 \cdot \text{rad}}{\text{sec}} t \right) \]
\[ v_E(t) = v_B(t) - 0.7 \cdot V \]

\[ \frac{R_C}{R_E + r_e} = 3.902 \]

\[ r_e = 2.5 \cdot \Omega \]

\[ v_C \]

\[ \text{difference } \leq 0.7 \text{V} \]

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Input impedance: \( R_i = R_{B1} \parallel R_{B2} \parallel \beta (r_e + R_E) \)

Output impedance: \( R_o = R_C || r_o \)

Often neglected \( r_o = \frac{V_A}{I_C} \) Early voltage (guess \( V_A = 100 \text{ V} \) if no data)

AC collector resistance: \( r_c = R_C || R_L || r_o \)

More correct, use: \( r_o = \frac{A_v}{A_v + 1} \)

instead of \( r_o \) very rarely done.

Voltage gain: \( A_v = \frac{v_o}{v_b} = \frac{r_c}{r_e + R_E} \)

Current gain: \( A_i = \frac{i_o}{i_i} = \frac{r_c R_L}{r_e + R_E R_L} = A_v \frac{R_L}{R_L} \)

Low frequency corner frequencies:

\( f_{CL1} = \frac{1}{2\pi (R_S + R_L) C_{in}} \)

\( f_{CL2} = \frac{1}{2\pi (R_L + R_o) C_{out}} \)

With bypass capacitor \( (C_E) \)

This basically makes the \( R_E \) dissapear at signal frequencies (If the cap is big enough).

Input impedance: \( R_i = R_{B1} || R_{B2} || \beta r_e \) Much lower

Output impedance: \( R_o = R_C || r_o \) Same as above, but no \( r_o \) correction needed

AC collector resistance: \( r_c = R_C || R_L || r_o \)

Voltage gain: \( A_v = \frac{v_o}{v_b} = \frac{r_c}{r_e} \)

Current gain: \( A_i = A_v \frac{R_L}{R_L} \)

Another low frequency corner frequency:

\( f_{CL3} = \frac{1}{2\pi C_E \left( \frac{1}{r_e} + \frac{1}{R_E} \right)} \)

Because \( r_e \) is so small, this will usually dominate, even when \( C_L \) is big.

If the output swing is too big you'll get distortion because \( r_o \) varies with \( I_C \)
High-frequency response

In general, capacitors that are placed in the circuit intentionally, those you can see, cause low-frequency poles. The unseen capacitors inside the parts and between the leads and the board traces cause high-frequency poles. These unseen capacitors have many names. Your textbook uses $C_p$ and $C_{\mu}$.

This capacitance causes the most trouble in common-emitter amplifiers because of it's location. It is connected between the input and the output, so it's effects are multiplied by the voltage gain. (The miller effect.)

$$f_T = \frac{1}{2\pi (C_{\pi} + C_{\mu}) r_e} = \text{freq. where } \beta \approx 1$$

**Input circuit model**

$$f_{CH1} = \frac{1}{2\pi C_{\pi} \left( \frac{1}{R_s} + \frac{1}{R_{in}} \right)}$$

**Miller Effect**

In a common-emitter amplifier:

$$v_c = -|A_v| v_b$$

$$i_{C_{\mu}} = \frac{v_b - v_c}{i + \omega C_{\mu}} = \left( v_b - \left( |A_v| v_b \right) \right) \left( i + \omega C_{\mu} \right)$$

$$= v_b \left( 1 + |A_v| \right) \left( i + \omega C_{\mu} \right)$$

If you wanted to make an equivalent amount of current flow to ground, you'd need a capacitor that was $(1+|A_v|)$ times as big. This is the Miller effect.

**Input circuit model**

$$f_{CH} = \frac{1}{2\pi \left[ C_{\pi} + C_{\mu} \left( 1 + |A_v| \right) \right] \left( \frac{1}{R_s} + \frac{1}{R_{in}} \right)}$$

The Miller effect will amplify any capacitance between the base and the collector, not just the capacitance within the transistor, so place leads and circuit traces carefully. If you're modeling a circuit in SPICE you'll have to model these "stray" capacitances if you want your high-frequency results to be any good.
Example:

Use $V_{m}=0.7, \beta=100, V_T=25\text{mV}$ (Vs is an ac source), ignore $r_e$.

Will this circuit work as an amplifier? Why or why not?

Example:

$V_2 = 0.1\text{mV}\sin(\omega t)$ and $\beta$ can vary from 20 to 200. The circuit shown below is suppose to amplify but does not. You expect the output at $V_o$ to amplify $V_2$. When you are testing the circuit, you find that it does not amplify. Explain why it does not and what exact resistor can be changed to allow it to amplify. It is not an ideal current source and can have a voltage drop across it.

\[ V_B = 5\text{V} \]
\[ V_C \approx 0\text{V} \]

Not in active region. Therefore, it will not amplify.

Need to decrease $R_4$ so that $V_c > V_B > V_E$. 

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Example

\[ V_0 = -g_m \frac{V_{be1}}{(1k \parallel 1k)} \]

\[ i = \frac{V_s}{R_{in}} = \frac{V_i V_m}{\beta H V_s} \]

\[ V_{be} = + \frac{r_m}{\beta H} = -0.39 V_s \]

\[ V_{be} = -\frac{r_m}{\beta H} \cdot \frac{V_s}{R_{in}} \]

\[ V_0 = -g_m \left( -\frac{r_m}{\beta H} \right) \frac{V_s}{R_{in}} (300) \]

\[ \frac{V_o}{V_s} = -2m \left( -\frac{10K}{81} \right) \frac{500}{1000} = 0.3 \frac{V}{V} \]

Using voltage divider:

\[ V_e = \frac{V_{in} + \frac{2K}{\beta + 1} V_s}{(V_{in} + 2K) + \frac{r_m}{\beta H} + \frac{1}{100}} = 0.35 V_s \]

\[ V_b = \frac{\frac{2K}{\beta + 1} - V_e}{\frac{r_m}{\beta H} + \frac{2K}{\beta + 1}} = -1.66 V_e = 0.058 V_s \]

\[ V_{be} = V_b - V_e = -0.29 V_s \]
Example:

Use $|V_{bb}|=0.7$, $V=2.5mV$ (Vs is an ac source), ignore $r$.

This small-signal model circuit is drawn below. The original circuit is also shown below. It was found through a DC analysis that $I_C=50\mu A$ and $I_{CE}=25\mu A$.

(a) Find the ac parameters

\[ P_{ac} = \frac{P_{dc}}{2} \]

(b) Find that input resistance, $R_{in}$ (ignore the AC input source $V_s$. include the 100 ohm) (12 points)

(c) Find the output resistance, $R_{out}$ (ignore the load resistor of 1k to the right of arrow) (6 points)

(d) Find the overall gain, $V_{out}/V_{in}$ (25 points)

Example:

A) $I_{b1} = \frac{I_{b1}}{k_1} = 3.5\mu A$

$R_{b1} = \frac{R_{b1}}{k_1} = (R_1) \frac{V_{bb}}{I_{b1}}$

$\delta_b = \frac{V_{bb}}{R_1}$

$g_{m1} = \frac{I_{b1}}{V_{bb}}$

$g_{m2} = \frac{I_{b3}}{V_{bb}}$

$g_{m3} = \frac{I_{b3}}{V_{bb}}$

$R_{out} = 100 + R_{b2} + 571 = 1622Ohm$

$R_{in} = 1k$ 

Result: $g_{m2}$ becomes open so that the 1k tied to it is floating.

---

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Example:

Use $|V_{BE}|=0.7$, $\beta=100$, $V_i=25\text{mV}$ ($V_2$ is an ac source).

- Find the DC values for the following
  a. $I_{RE}$ (15 points)
  b. $I_{C1}$ (3 points)
  c. $V_{RE}$ (6 points)
  d. $V_{C1}$ (6 points)
  e. $V_{BE}$ (5 points)

\[ \text{Thévenin of } R_1 \text{ and } R_2: \]

\[ V_{TH} = V_{BC} = 37.5 \text{V} \]

\[ 37.5 = \frac{V_{TH}}{2k} + I_{C} \]

\[ I_{C} = \frac{V_{TH}}{2k} \]

\[ I_{E} = \frac{I_{C}}{\beta} \]

\[ I_{E} = 1.3\text{mA} \]

\[ V_{E} = I_{E} (3k) - 10 = -6.1 \]

\[ I_{C} = \alpha I_{E} = 1.20 \text{mA} \]

\[ V_{B} = V_{TH} - I_{B} (R_2) = 2.4 \text{V} \]

\[ I_{B} = 12.9 \mu\text{A} \]

\[ V_{C} = 10 - I_{C} (3k) = 8.74 \]

\[ V_{C} > V_{B} > V_{E} \]

**Special multiple-transistor connections.**

*Often wired together in a single package*

**Darlington**

For the pair taken together:

\[ V_{BE} = 1.4 \text{V} \]

\[ \beta = \beta_1 \cdot \beta_2 \]

Saturation:

\[ V_{CE} = 0.9 \text{V} \]

R is often added to improve the turn-off speed.

**Sziklai**

For the pair taken together:

\[ V_{BE} = 0.7 \text{V} \]

\[ \beta = \beta_1 \cdot \beta_2 \]

Saturation:

\[ V_{CE} = 0.9 \text{V} \]