ECE 2100 Lecture Notes 4/18/03

Stuff Review for Final: Fri, 4/25 3:30 pm
Final: Mon, 4/28 8:00 am

Spice #S3, due: F, 4/18 handout

HW # 23, due: F 4/18 Ex5.17 - Ex5.23
May be handed in Monday because I screwed up

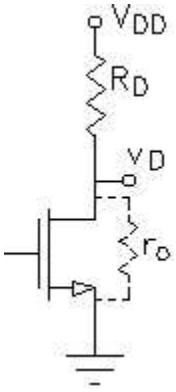
HW # 24, due: M 4/21 Ex5.24 - Ex5.34
Ex 5.28 Book answers are OK
May need for Ex5.33: V_{DD}= 5V, V_{tn}= 0.8V

HW # 25, due: W 4/23 Ex5.35 - Ex5.39

HW # 26, due: W 4/23 Ex5.40 - Ex5.48
May be handed in with the final

N-channel MOSFETs as R_D in CS amp p.419

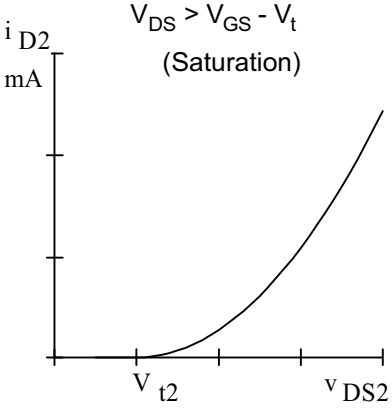
Basic CS Amp

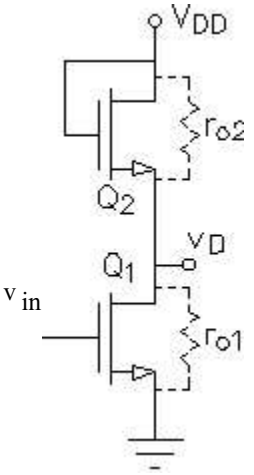


Last time we replaced the R_D with a current source made with P-channel devices and got a good amplifier, But PMOS devices take up a lot of space on an IC.

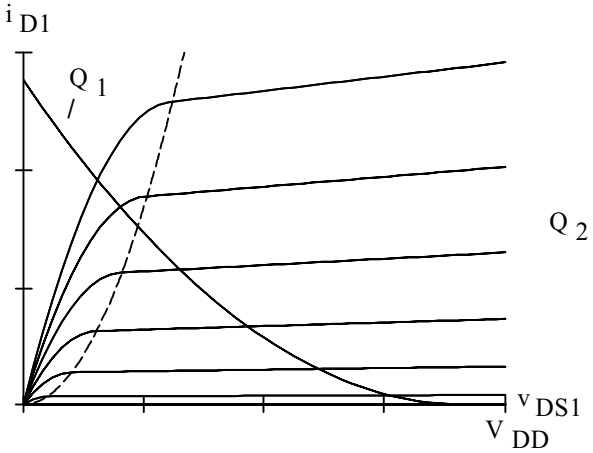
Try a new configuration using an NMOS with the drain connected to the gate.

Q_2 is guaranteed to be in saturation because $V_D = V_G$. Also, it's $V_{GS} = V_{DS}$, so we can draw the following familiar curve with a new x-axis variable:





If I draw the curve with respect to $V_{DD} - V_{DS2} = V_{DS1}$, it will go backwards and can now be drawn on top of the Q_1 curves:



Notice that the new "load line" curves up. Its non-linearity will nicely offset the inherent i_D vs v_{GS} non-linearity of the Q_1. This results in a very linear transfer characteristic and an unexpected square root in the gain term. Too bad the gain stinks.

$$i_{D1} = \frac{1}{2}\cdot k'_n\cdot\frac{W_1}{L_1}\cdot\left(V_{GS}+v_{in}-V_{t1}\right)^2 = i_{D2} = \frac{1}{2}\cdot k'_n\cdot\frac{W_2}{L_2}\cdot\left(V_{DD}-V_D-v_o-V_{t2}\right)^2$$

$$\sqrt{\frac{W_1}{L_1}\cdot\left(V_{GS}+v_{in}-V_{t1}\right)^2} = \sqrt{\frac{W_2}{L_2}\cdot\left(V_{DD}-V_D-v_o-V_{t2}\right)^2}$$

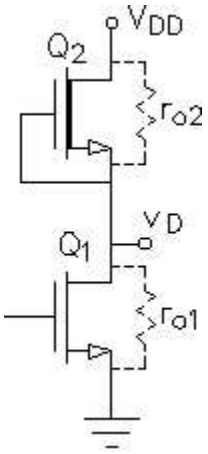
$$\sqrt{\frac{W_1}{L_1}\cdot\frac{L_2}{W_2}}\cdot\left(V_{GS}+v_{in}-V_{t1}\right) = \left(V_{DD}-V_D-v_o-V_{t2}\right)$$

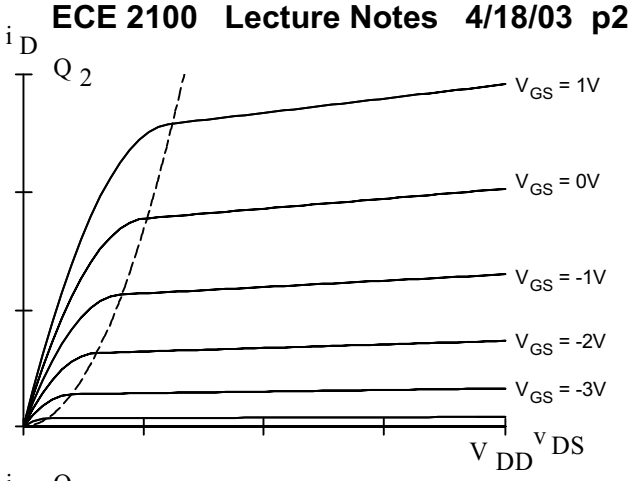
Subtract off the constant, bias values from both sides: $A_v = \frac{v_o}{v_{in}} \simeq -\sqrt{\frac{W_1\cdot L_2}{L_1\cdot W_2}}$

If you account for the body effects of Q_2: $A_v = -\sqrt{\frac{W_1\cdot L_2}{L_1\cdot W_2}}\cdot\left(\frac{1}{1+\chi}\right)$

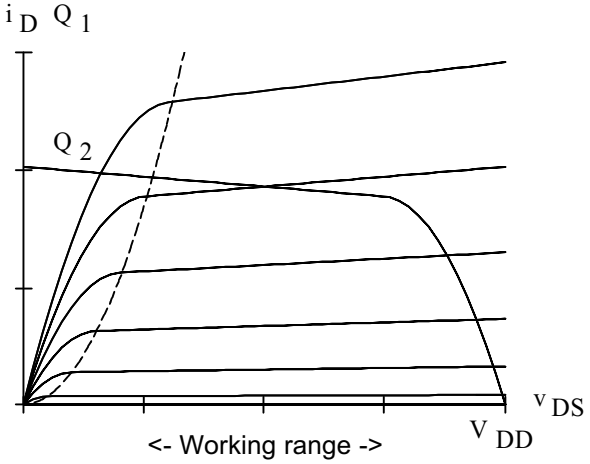
Depletion-type MOSFET as R_D p.421

The connection of Q_2's drain to its gate insured that it was in the saturation region. The same connection will not have the same effect on a depletion-type NMOS. Because these parts have a negative V_t , V_D must be $-V_t$ volts higher than the gate. This is not a bad thing, because now we'll get a current flow even with $v_{GS} = 0$. That means that we can tie the gate to the source and simply operate on the $v_{GS} = 0$ curve.



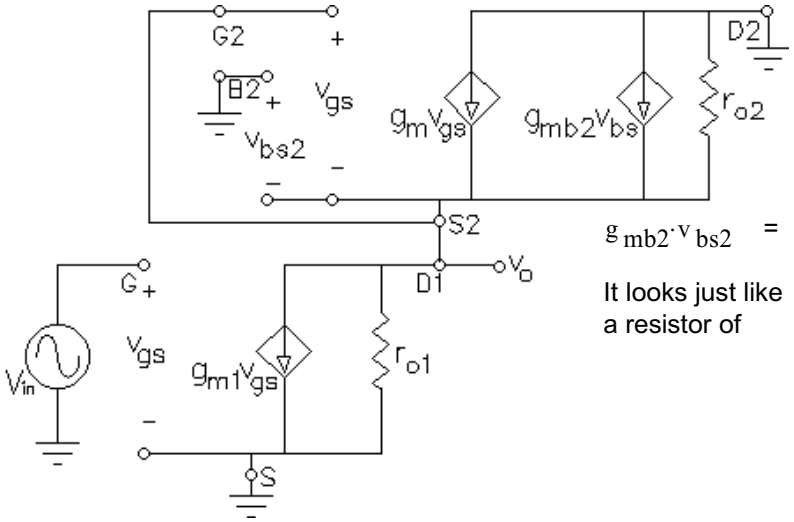


If I draw the $v_{GS} = 0$ curve with respect to $V_{DD} - V_{DS2} = V_{DS1}$, it will go backwards and can now be drawn on top of the Q_1 curves:



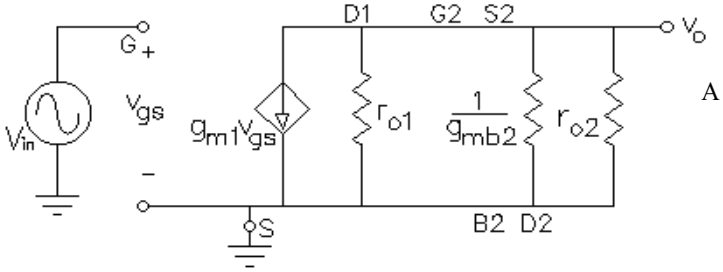
<- Working range ->

This looks an awful lot like the PMOS load, but it's much different because of Q_2 body effects.



$$g_{mb2} \cdot v_{bs2} = g_{mb2} \cdot (-v_o)$$

It looks just like a resistor of $\dfrac{1}{g_{mb2}}$

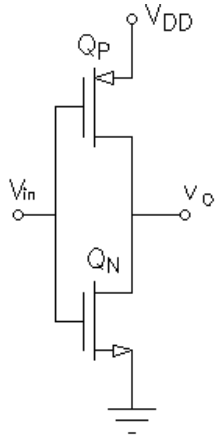


$$A_v = -g_{m1} \cdot \frac{1}{g_{mb2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}}} \simeq -\frac{g_{m1}}{g_{mb2}} = -\frac{g_{m1}}{\chi \cdot g_{m2}}$$

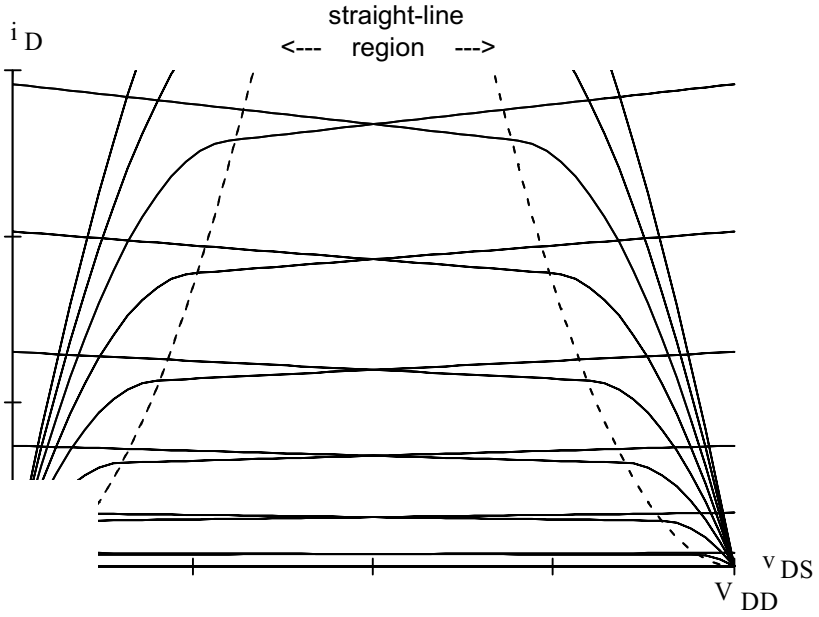
Since: $g_m = \sqrt{k'_n \cdot \frac{W}{L} \cdot 2 \cdot I_D}$ and both transistors share the same i_D,

$$A_v = -\sqrt{\frac{W_1 \cdot L_2}{L_1 \cdot W_2}} \cdot \left(\frac{1}{\chi}\right)$$

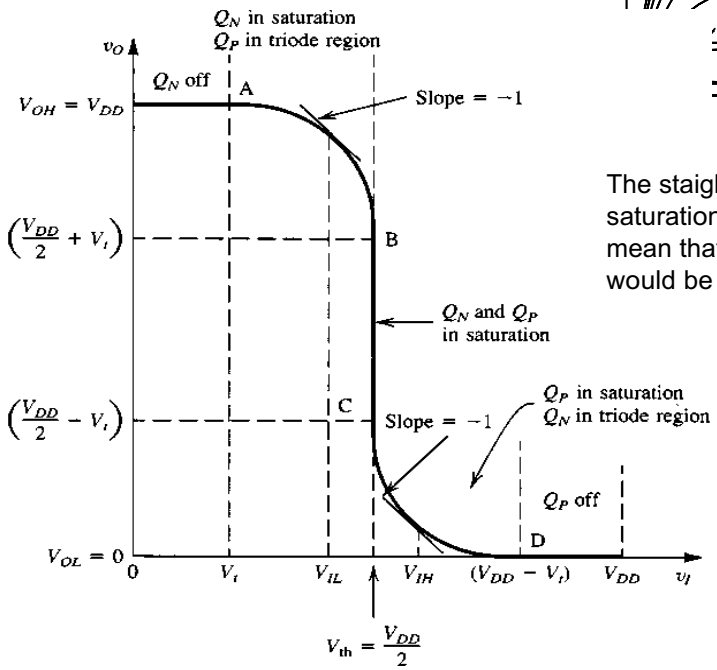
Which is about 3 times higher than the previous circuit.



$V_{DD} = V_{GS2} + V_{GS1}$ If I draw the $v_{GS} = 0$ curve with respect to V_{DD} - $V_{DS2} = V_{DS1}$, it will go backwards and can now be drawn on top of the Q_1 curves:



The staight-line region, where both transistors are in saturation would only be verical if $\lambda = 0$, that would mean that the saturation part of the curves above would be flat. Not a real possibility.



Right in the center (V_{th})

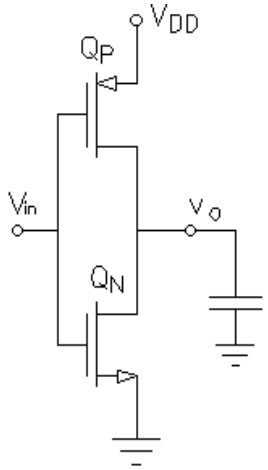
As a digital inverter, when the output is high, v_{ds} for the p-channel part is small and the output resistance looks like the r_{ds} for that transistor.

When the output is low, v_{ds} for the n-channel part is small and the output resistance looks like the r_{ds} for that transistor.

$$r_{ds} = \frac{1}{k'_n \cdot \frac{W}{L} \cdot \left(V_{DD} - |V_t|\right)}$$

$$i_{Dn} = i_{Dp}$$

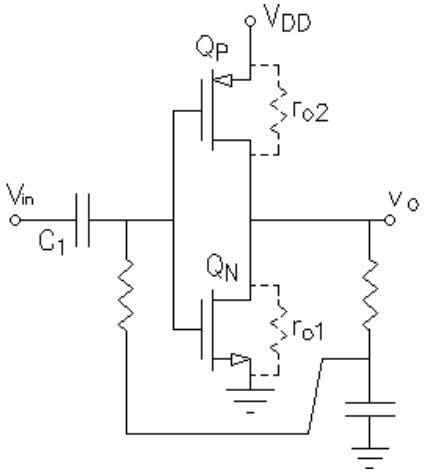
$$i_{Dn} = \frac{1}{2} \cdot k'_n \cdot \frac{W_n}{L_n} \cdot \left(V_{th} - V_{tn}\right)^2 = i_{Dp} = \frac{1}{2} \cdot k'_p \cdot \frac{W_p}{L_p} \cdot \left(V_{DD} - V_{th} - |V_{tp}|\right)^2$$



CMOS Digital circuits are usually hooked to other MOS parts, so the load they see is usually a capacitor.

The text goes into some detail about how the capacitor is charged and discharged to find the rise and fall times. These times set the speed limits of the digital circuitry.

A full on-off cycle results in a finite amout of charge flowing ffirst from V_{DD} into the capacitor and then from the capacitor to ground. This means a certain amout aof energy is used for each cycle.



Also makes a good linear amplifier, with the right bias: