ECE 2100 Lecture Notes 4/16/03

A. Stolp
4/15/03,
4/17/03

Stuff Review for Final: Fri, 4/25 3:30 pm
Final: Mon, 4/28 8:00 am

HW # 22, due: W 4/16 Ex5.9 - Ex5.16
Check assumptions, esp saturation on 15 & 16

Spice #S3, due: F, 4/18 handout

HW # 23, due: F 4/18 Ex5.17 - Ex5.23

HW # 24, due: M 4/21 Ex5.24 - Ex5.34
Ex 5.28 Ans: ...128kΩ, 192kΩ,...
May need for Ex5.33: V_{DD}= 5V, V_{tn}= 0.8V

HW # 25, due: W 4/23 Ex5.35 - Ex5.39

HW # 26, due: W 4/23 Ex5.40 - Ex5.48

Current mirrors, continued

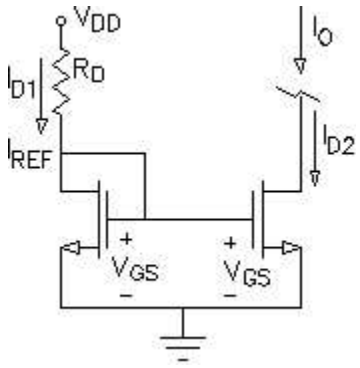
We have an equation to solve for I_D if $V_{GS} = V_G - R_S \cdot I_D$ but now...

To find I_{REF}, notice: $V_{GS} = V_{DD} - R_D \cdot I_{D1}$ adapt previous eq:

$$0 = \underbrace{R_D^2 \cdot I_{D1}^2}_{a} - 2 \cdot \underbrace{\left[\left(V_{DD} - V_t\right) \cdot R_D + \frac{1}{k'_n \cdot \frac{W}{L}} \right]}_{b} \cdot I_{D1} + \underbrace{\left(V_{DD} - V_t\right)^2}_{c}$$

$$I_{D1} = \frac{-b + \sqrt{b^2 - 4 \cdot a \cdot c}}{2 \cdot a} \quad \text{or} \quad I_{D1} = \frac{-b - \sqrt{b^2 - 4 \cdot a \cdot c}}{2 \cdot a} = I_{REF}$$

Only one of which will make sense. ($V_{GS} > V_t$).



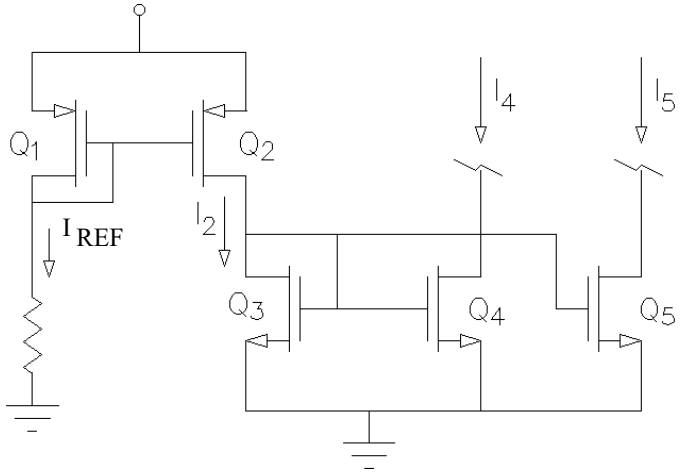
One current source could be the reference for another current source...

Each Mosfet can have a different W/L

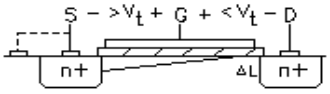
$$\frac{I_2}{I_{REF}} = \frac{W_2}{L_2} \cdot \frac{L_1}{W_1} \quad \text{if all have same } k'_n$$

$$\frac{I_4}{I_{REF}} = \frac{W_4}{L_4} \cdot \frac{L_3}{W_3} \cdot \left(\frac{W_2}{L_2} \cdot \frac{L_1}{W_1} \right)$$

$$\frac{I_5}{I_{REF}} = \frac{W_5}{L_5} \cdot \frac{L_3}{W_3} \cdot \left(\frac{W_2}{L_2} \cdot \frac{L_1}{W_1} \right)$$

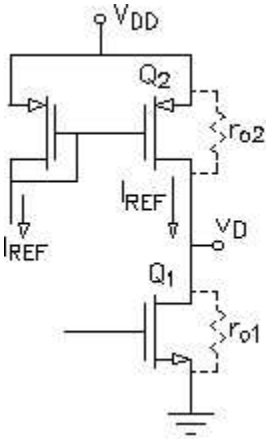


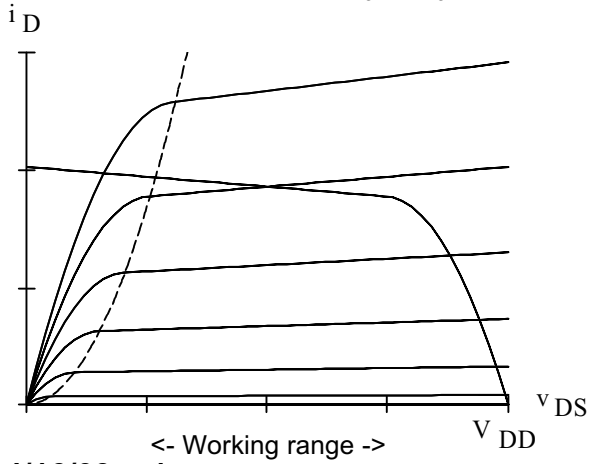
Want current to be independent of voltage, r_o should be very large, so:



Make channel length long

Common source biased with current mirror p.410





<- Working range ->

$$r_d = \frac{1}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}}} \quad \text{or} \quad r_d = \frac{1}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{1}{R_L}}$$

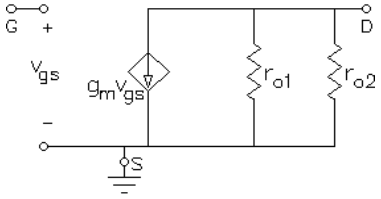
load line slope = $-\frac{1}{r_d}$

voltage gain

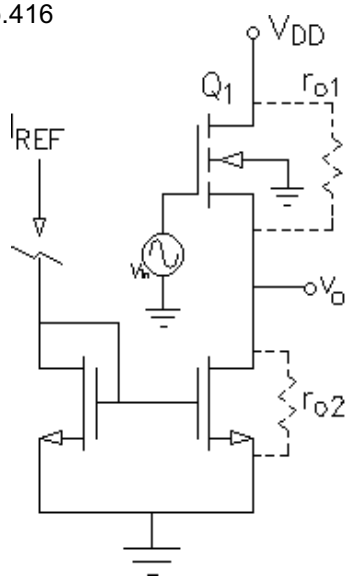
$A_V = g_m \cdot r_d$

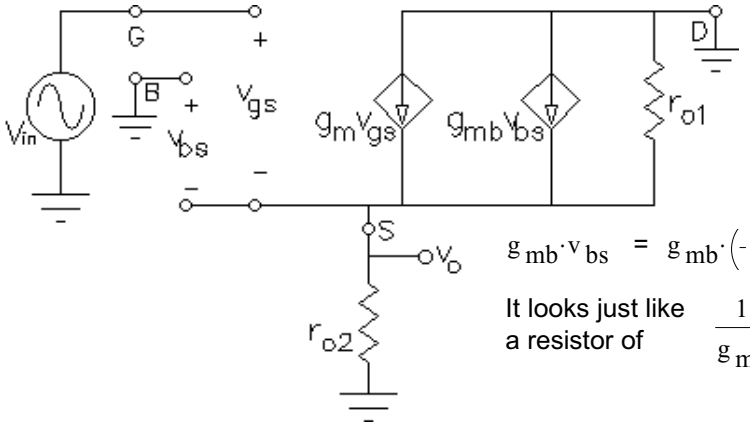
Good gain, 20 to 100

But lousy R_o (high)



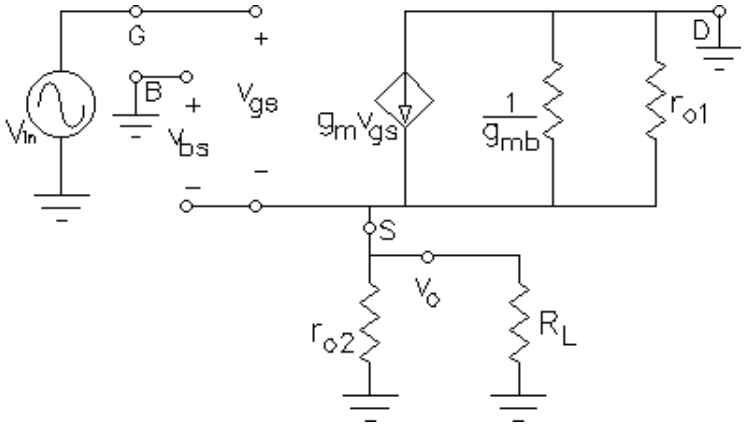
p.416

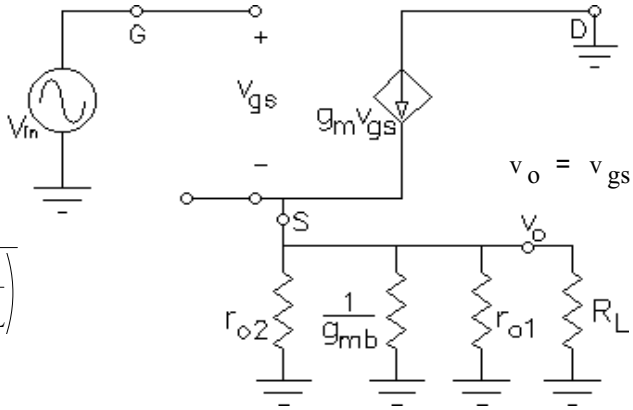




$g_{mb} \cdot v_{bs} = g_{mb} \cdot (-v_o)$

It looks just like a resistor of $\frac{1}{g_{mb}}$





Define

$$R'_S = \frac{1}{\left(g_{mb} + \frac{1}{r_{o2}} + \frac{1}{r_{o1}} + \frac{1}{R_L}\right)}$$

$$v_o = v_{gs} \cdot g_m \cdot \frac{1}{\left(g_{mb} + \frac{1}{r_{o2}} + \frac{1}{r_{o1}} + \frac{1}{R_L}\right)}$$

$$v_o = v_{gs} \cdot g_m \cdot R'_S$$

$$= (v_{in} - v_o) \cdot g_m \cdot R'_S = v_{in} \cdot g_m \cdot R'_S - v_o \cdot g_m \cdot R'_S$$

$$\frac{v_o}{v_{in}} = \frac{g_m \cdot R'_S}{1 + g_m \cdot R'_S} = \frac{g_m}{\frac{1}{R'_S} + g_m} = \frac{g_m}{g_m + \left(g_{mb} + \frac{1}{r_{o2}} + \frac{1}{r_{o1}} + \frac{1}{R_L}\right)} = \frac{g_m}{g_m + \chi \cdot g_m + \frac{1}{r_{o2}} + \frac{1}{r_{o1}} + \frac{1}{R_L}}$$

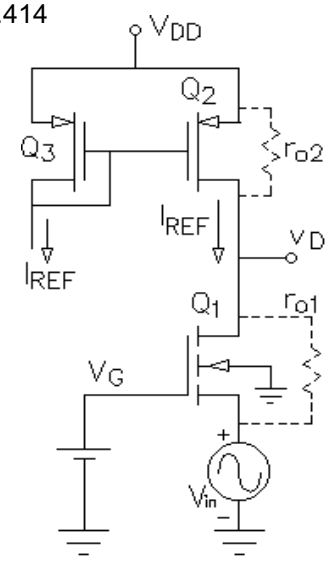
To find R_o, zero v_{in}, then you'll notice that $v_{gs} = v_{bs}$, so by the same type of analysis used on g_{mb}, $1/g_m$ just looks like another resistor in parallel with $1/g_{mb}$.

$$R_o = \frac{1}{\left(g_m + g_{mb} + \frac{1}{r_{o2}} + \frac{1}{r_{o1}}\right)}$$

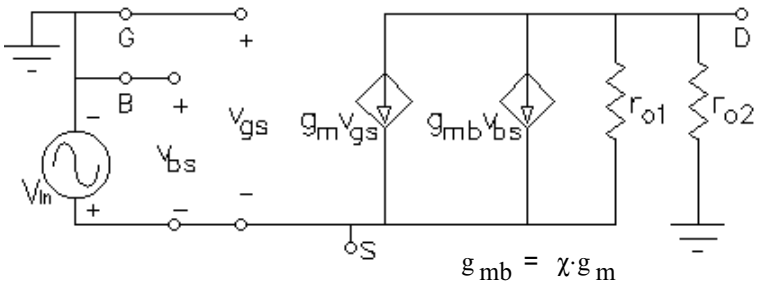
often neglected /____/

The input is into the gate, so: $R_{in} = \infty$ At low enough frequencies that the input capacitance isn't a problem.

p.414

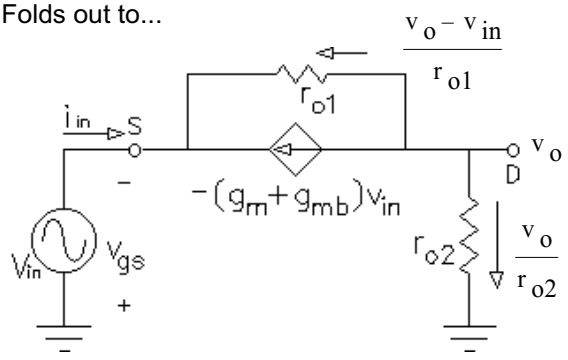


Source is the signal input, so let's assume the body is hooked to ground. Gate is at signal ground, so..



$g_{mb} = \chi \cdot g_m$

Folds out to...



Good gain, 20 to 100

But lousy R_{in} & R_o

Like common base amp, has no Miller effect, so is good at high frequencies.

Is usually part of a two part amplifier, like a cascode or differential amp

KCL at D: $\left(g_m + g_{mb}\right)\cdot v_{in} = \frac{\left(v_o - v_{in}\right)}{r_{o1}} + \frac{v_o}{r_{o2}} = \frac{v_o}{r_{o1}} - \frac{v_{in}}{r_{o1}} + \frac{v_o}{r_{o2}}$

$$\left(g_m + g_{mb} + \frac{1}{r_{o1}}\right)\cdot v_{in} = v_o \cdot \left(\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{1}{R_L}\right)$$ adding a term for a possible R_L

$$A_V = \frac{v_o}{v_{in}} = \left(g_m + g_{mb} + \frac{1}{r_{o1}}\right) \cdot \frac{1}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{1}{R_L}}$$

often neglected /

R_{in}, p.415 derivation below is not required

$$i_{in} = \left(g_m + g_{mb}\right)\cdot v_{in} + \frac{\left(v_{in} - v_o\right)}{r_{o1}} = \left(g_m + g_{mb}\right)\cdot v_{in} + \frac{v_{in}}{r_{o1}} - \frac{v_o}{r_{o1}} = \left(g_m + g_{mb} + \frac{1}{r_{o1}}\right)\cdot v_{in} - \frac{v_o}{r_{o1}}$$

$$= \left(g_m + g_{mb} + \frac{1}{r_{o1}}\right)\cdot v_{in} - \frac{A_v \cdot v_{in}}{r_{o1}} = \left[\left(g_m + g_{mb} + \frac{1}{r_{o1}}\right) - \frac{A_v}{r_{o1}}\right]\cdot v_{in}$$

$$= \left[\left(g_m + g_{mb} + \frac{1}{r_{o1}}\right) - \frac{\left(g_m + g_{mb} + \frac{1}{r_{o1}}\right)\cdot \frac{1}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{1}{R_L}}}{r_{o1}}\right]\cdot v_{in} = \left(g_m + g_{mb} + \frac{1}{r_{o1}}\right)\cdot\left[1 - \frac{1}{\frac{r_{o1}}{r_{o1}} + \left(\frac{1}{r_{o2}} + \frac{1}{R_L}\right)\cdot r_{o1}}\right]\cdot v_{in}$$

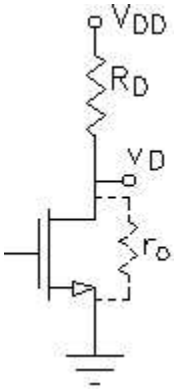
$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{\left(g_m + g_{mb} + \frac{1}{r_{o1}}\right)} \cdot \frac{1}{\left[1 - \frac{1}{1 + \left(\frac{1}{r_{o2}} + \frac{1}{R_L}\right)\cdot r_{o1}}\right]} = \frac{1}{\left(g_m + g_{mb} + \frac{1}{r_{o1}}\right)} \cdot \frac{1 + \left(\frac{1}{r_{o2}} + \frac{1}{R_L}\right)\cdot r_{o1}}{\left[1 + \left(\frac{1}{r_{o2}} + \frac{1}{R_L}\right)\cdot r_{o1} - 1\right]}$$

$$= \frac{1}{\left(g_m + g_{mb} + \frac{1}{r_{o1}}\right)} \cdot \frac{1 + \left(\frac{1}{r_{o2}} + \frac{1}{R_L}\right)\cdot r_{o1}}{\left[\left(\frac{1}{r_{o2}} + \frac{1}{R_L}\right)\cdot r_{o1}\right]} = \frac{1}{\left(g_m + g_{mb} + \frac{1}{r_{o1}}\right)} \cdot \left[\frac{1}{\left(\frac{1}{r_{o2}} + \frac{1}{R_L}\right)\cdot r_{o1}} + 1\right]$$

Compare to eq. 5.65

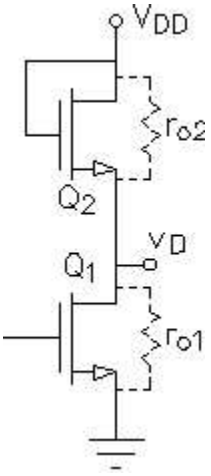
often neglected /

Basic CS Amp



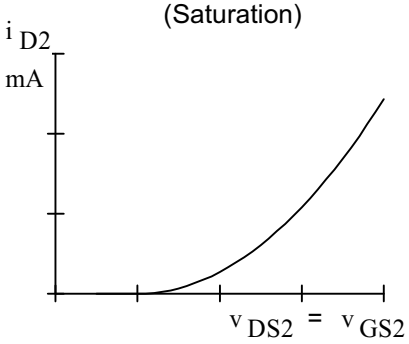
Last time we replaced the R_D with a current source made with P-channel devices and got a good amplifier, But PMOS devices take up a lot of space on an IC.

Try a new configuration using an NMOS with the drain connected to the gate.

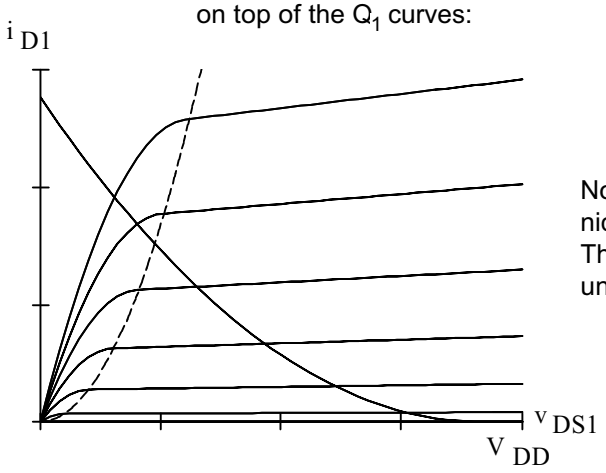


Q_2 is guaranteed to be in saturation because $V_D = V_G$. Also, it's $V_{GS} = V_{DS}$, so we can draw the following familiar curve with a new x-axis variable:

$V_{DS} > V_{GS} - V_t$ (Saturation)



If I draw the curve with respect to $V_{DD} - V_{DS2} = V_{DS1}$, it will go backwards and can now be drawn on top of the Q_1 curves:

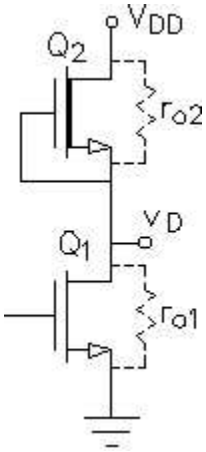


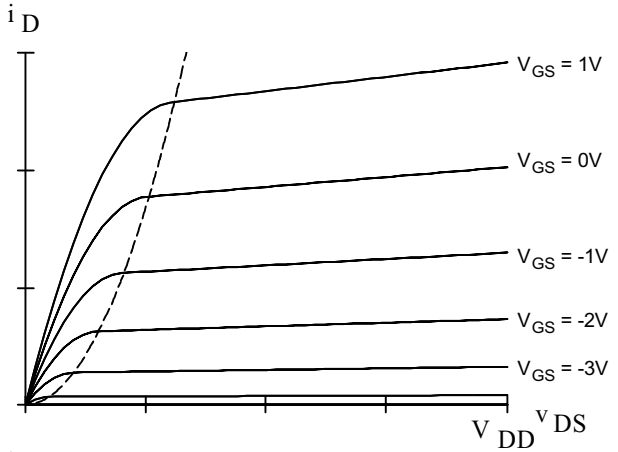
Notice that the new "load line" curves up. Its non-linearity will nicely offset the inherent i_D vs v_{GS} non-linearity of the Q_1. This results in a very linear transfer characteristic and an unexpected sq root in the gain term. Too bad the gain stinks.

$$A_v \tilde{-} -\sqrt{\frac{W_1 \cdot L_2}{L_1 \cdot W_2}}$$

Depletion-type MOSFET as R_D p.421

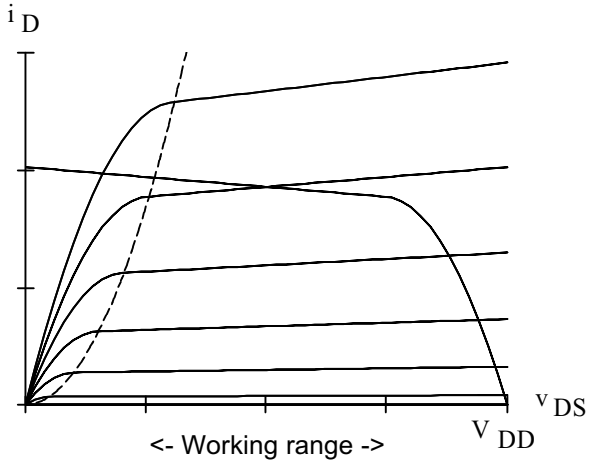
The connection of Q_2's drain to its gate insured that it was in the saturation region. The same connection will not have the same effect on a depletion-type NMOS. Because these parts have a negative V_t , V_D must be $-V_t$ volts higher than the gate. This is not a bad thing, because now we'll get a current flow even with $v_{GS} = 0$. That means that we can tie the gate to the source and simply operate on the $v_{GS} = 0$ curve.





If I draw the $v_{GS} = 0$ curve with respect to $V_{DD} - V_{DS2} = V_{DS1}$, it will go backwards and can now be drawn on top of the Q_1 curves:

This look an awful lot like the PMOS load, but it's a little bit strange because of Q_2 body effects.



<- Working range ->