ECE 2100 Lecture Notes 4/14/03

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4/13/03

HW # 22, due: W 4/16 Ex5.9 - Ex5.16
Check assumptions, esp saturation on 15 & 16

Spice #S3, due: F, 4/18 handout

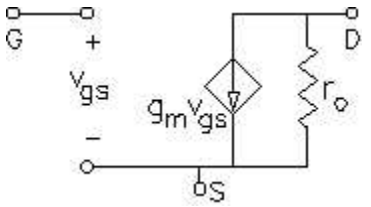
HW # 23, due: F 4/18 Ex5.17 - Ex5.23

HW # 24, due: M 4/21 Ex5.24 - Ex5.34
Ex 5.28 Ans: ...128kΩ, 192kΩ,...
May need for Ex5.33: V_{DD}= 5V, V_{tn}= 0.8V

HW # 25, due: W 4/23 Ex5.35 - Ex5.39

Small signal Model

MOSFET



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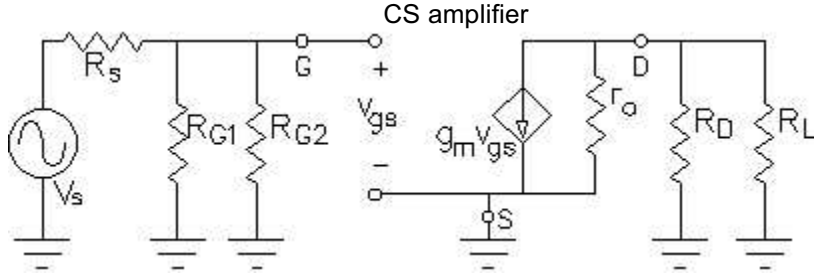
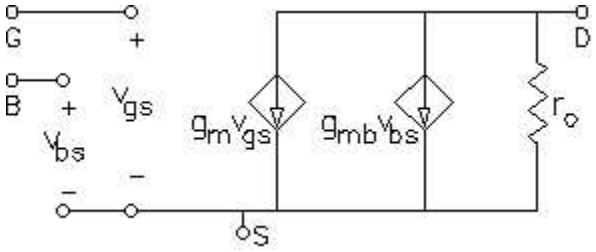
CS amplifier



Body Effect (small signal) Treat body as a second gate, and so as a second input p399.



$g_{mb} = \chi \cdot g_m$ typ: $0.1 \cdot g_m$ to $0.3 \cdot g_m$

$\chi = \dfrac{\gamma}{2 \cdot \sqrt{2 \cdot \phi_f + V_{SB}}}$ typ: $\gamma := 0.5 \cdot \sqrt{V}$

typ: $\phi_f := 0.3 \cdot V$ $2 \cdot \phi_f = 0.6 \cdot V$

bias

DC Body effects (repeated here for completeness)

V_t with no V_{SB}

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$$V_t = V_{t0} + \gamma \cdot \left(\sqrt{2 \cdot \phi_f + V_{SB}} - \sqrt{2 \cdot \phi_f} \right)$$

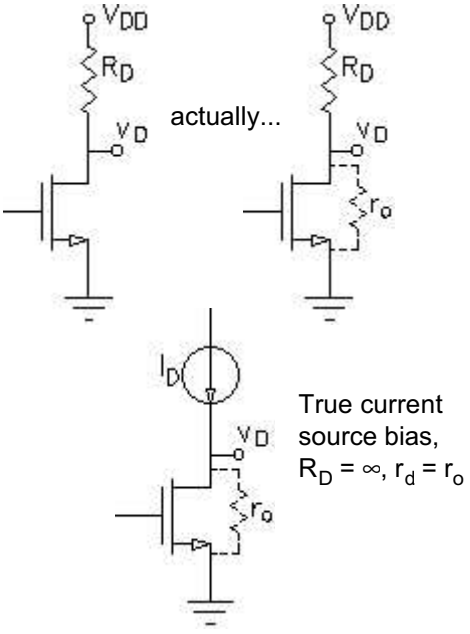
Body effect parameter: $\gamma = \dfrac{\sqrt{2 \cdot q \cdot N_A \cdot \varepsilon_s}}{C_{ox}}$

Permittivity of silicon: $\varepsilon_s := 1.035 \cdot 10^{-12} \cdot \dfrac{F}{cm}$

Electron charge: $q := 1.60 \cdot 10^{-19} \cdot coul$

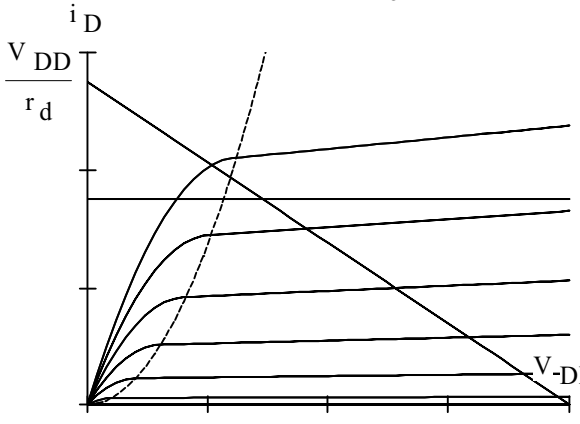
N_A =doping of p substrate

Load lines



True current source bias, $R_D = \infty$, $r_d = r_o$

$$r_d = \frac{1}{\frac{1}{R_D} + \frac{1}{r_o}} \quad \text{or} \quad r_d = \frac{1}{\frac{1}{R_D} + \frac{1}{r_o} + \frac{1}{R_L}}$$



load line slope = $-\dfrac{1}{r_d}$

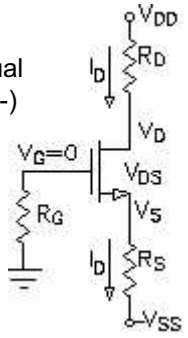
voltage gain

$A_V = g_m \cdot r_d$

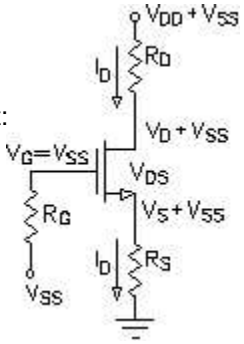
True current source, flat line, Av = ∞

Other bias methods

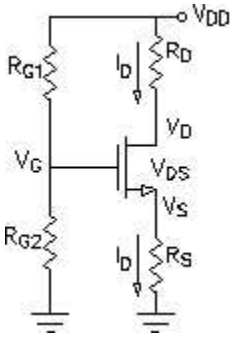
If you have dual supplies (+ & -)



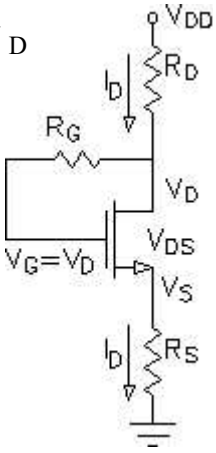
I usually like to use this little analysis trick of "lifting" the whole circuit:



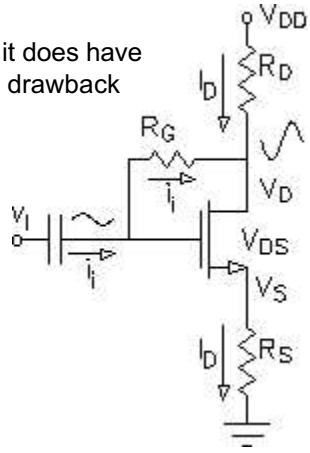
Then it looks a lot like the circuit I've already analyzed & I can use the same equations with very little modification.



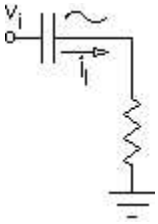
$V_G = V_D$ simple



But it does have one drawback



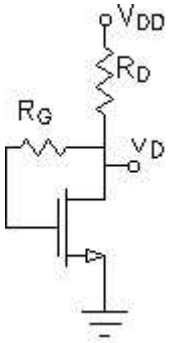
R_{in} is much smaller than R_G because of the Miller effect



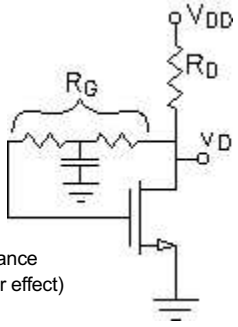
$$R_{in} = \frac{R_G}{(A_v + 1)}$$

p396

You really don't need R_S.



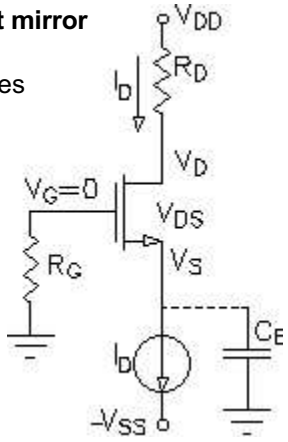
or...



Better input Impedance
(Short-out the Miller effect)

Current source bias from current mirror

Most common bias in ICs involves a current source

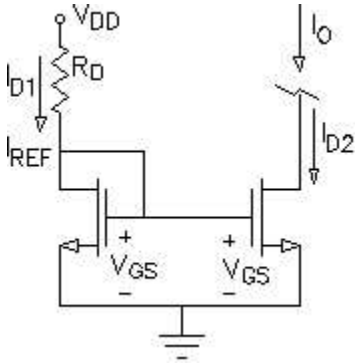


Note this particular arrangement doesn't have voltage gain unless the current source is bypassed, a rare thing in ICs since capacitors are so expensive to make in silicon.

Usually the current source is in a different position.

Current mirrors

$$I_{D1} = \frac{1}{2} \cdot k'_n \cdot \frac{W_1}{L_1} \cdot (V_{GS} - V_t)^2$$



$$I_{D2} = \frac{1}{2} \cdot k'_n \cdot \frac{W_2}{L_2} \cdot (V_{GS} - V_t)^2$$

The same VGS can be used to turn on many current sources, each with its own W/L ratio.

Usually k'_n and V_t are the same for both MOSFETs because they are in the same IC and were made by same processing, but you can still adjust the I_O current to any value you want by adjusting the W/L ratios.

$$\frac{I_O}{I_{REF}} = \frac{W_2}{L_2} \cdot \frac{L_1}{W_1}$$