Electrical & Computer Engineering
ECE 2100
Experiment No. 12
MOSFET Circuits

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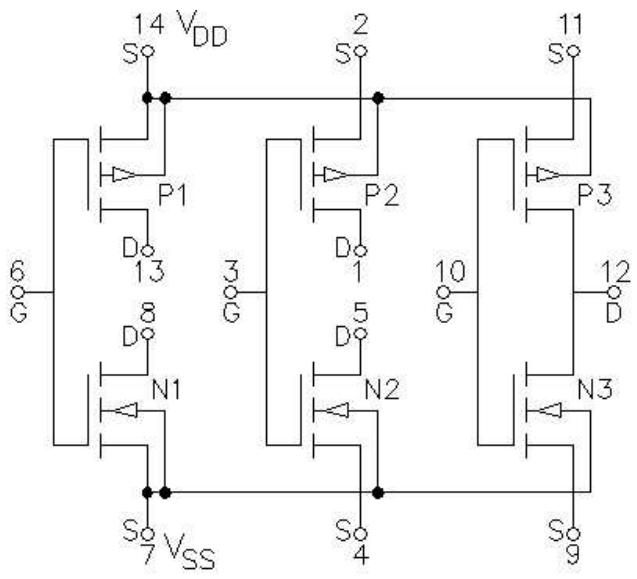
rev, 4/6/03

Bring your textbook to lab.

Minimum required points = 40
Recommend parts (all) = 57 pts (100%)

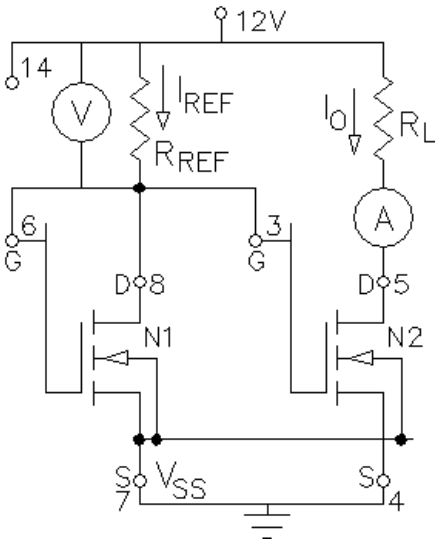
Objectives
1. Build and test a current mirror circuit.
2. Explore analog switch circuits.

Check out from stockroom:
- Wire kit & 10x scope probes
- DC ammeter or multimeter
- Second signal generator or use one of the old benches. You can also use a second HP generator from a neighboring, bench. See if your neighbors will share for the last part of this lab.



CA3600 MOSFET Array
The CA3600 part that you use in this lab is expensive and easily damaged. Read the box in the last lab. Follow those procedures and heed those warnings.

Parts:
- four 1 kΩ, two 10 kΩ, & two 100 kΩ resistors
- CA3600 MOSFET array
- Proto-board and wires
- CMOS inverter (MC14069, CD4069 or any CMOS part that inverts like a NAND or NOR)
- 0.22 µF capacitor



Exp. 1, Current mirror (14 pts, Recommended)
Build the current mirror shown at right. If this looks a little complex, refer to Fig. 5.40, p.403 in your textbook for the simpler version. Use 1 kΩ resistors for R_{REF} and R_L. The voltmeter across R_{REF} will allow you to calculate the current, I_{REF}, and the ammeter will allow you to measure the "output" current. Don't forget the +12 V to pin 14 connection.

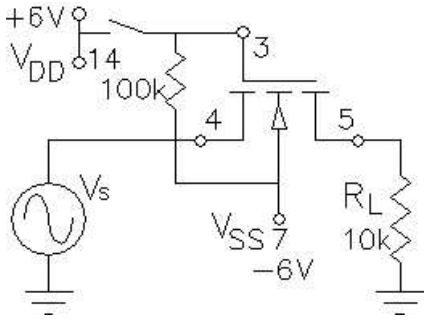
Turn on the power and determine I_{REF} and I_O, They should be close to the same value. If they're not, reread the first box in the last lab about the CA3600, check your circuit, and then try a different pair of transistors in the CA3600 part. If you can't find two working n-channel transistors, use two p-channel and adapt the circuit. Either way, make certain that pin 14 and 7 remain connected to the positive voltage supply and ground.

Record I_{REF} . Measure and record the "output" current (I_O) for several loads, R_L = 1kΩ, 500 Ω (two 1k's in parallel), and 0Ω (just the ammeter). Ideally, the load current will stay the same regardless of the value of the load resistor.

Now try a different I_{REF}. Change R_{REF} to 500 Ω (two 1k's in parallel), find and record the new I_{REF} . Measure and record I_O for R_L = 1kΩ, 500 Ω (two 1k's in parallel), and 0Ω (just the ammeter) again.

Current mirrors are commonly used in IC designs to provide bias currents. Comment on the workings of the current mirror in your notebook (as conclusion).

Exp. 2, Analog switches (22 pts, Recommended)

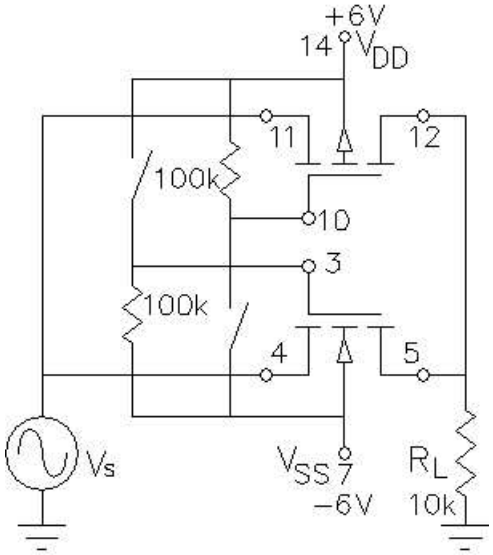


NMOS switch: Build the analog switch circuit shown at right. This is practically the same circuit shown in Fig. 5.62, p.437, with the addition of a 100 kΩ pull-down resistor and a switch (just use a wire in your proto-board). You must use either transistor N2 or N3 for this circuit. N1 won't work because its source is hooked to the body. Notice that the circuit requires ± 6 V supplies and don't forget the +6 V to pin 14 connection.

Using a small input signal from the signal generator, confirm that this analog switch works as expected, that is, when the gate voltage is high (switch closed), the signal appears at R_L and when the gate voltage is low (switch open), no signal appears at R_L.

Exchange the positions of the signal source (V_S) and the load resistor (R_L) (swap connections to pins 4 & 5). Does this analog switch circuit work just as well both ways? Return connections to where they were.

Increase the input signal amplitude until you see distortion at the output. What is the largest signal that this circuit can handle with no visible distortion? What causes this distortion? Hint: Are v_{GS} and V_{GD} constant throughout the waveform of v_S? The next circuit will eliminate most of this distortion problem.



CMOS Transmission gate: Build the circuit shown at right. This is practically the same circuit shown in Fig. 5.64, p.439, with the addition of pull-up and pull-down resistors and "switches" (just wire contacts in your proto-board). You must use either transistors N2 and P3 or N3 and P2 for this circuit. Other combinations won't work because of internal connections within the CA3600.

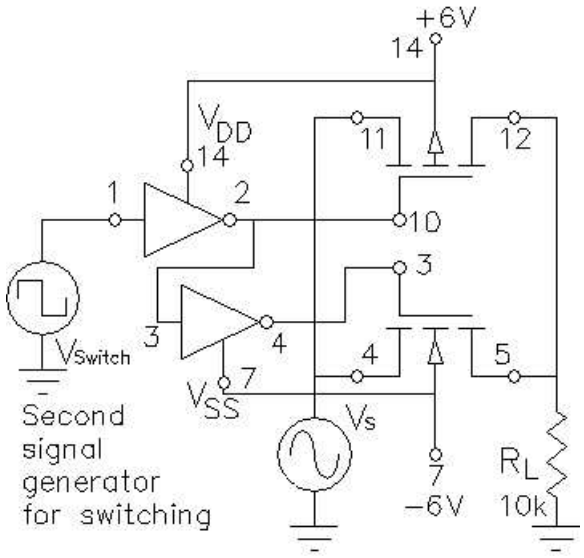
Using a small input signal, confirm that this transmission gate works as expected, that is, when both wire contacts are closed, the signal appears at R_L and when they're open, no signal appears at R_L.

Increase the input signal amplitude until you see

distortion at the output. DO NOT EXCEED 12 Vpp. What is the largest signal that this circuit can handle with no visible distortion? Compare this maximum to the maximum undistorted signal passable by the simple NMOS switch.

Exp. 3, Logically controlled Transmission Gate (21 pts, Recommended)

Remove the pull-up and pull-down resistors and add the CMOS inverter to the transmission gate circuit as shown. (A pin-out for the 4069 inverter shown at the bottom of this page. If you use different part, get other data.) Now the transmission gate can be controlled by the second signal generator (set to produce a square wave output of about ± 5 V).



Signal switch: When the frequency of V_S is higher than V_{Switch} the output appears to be V_S switched on and off. Play with the frequencies and the scope triggering. Make a sketch of the output and comment in your notebook.

Chopped signal: When the frequency of V_S is lower than V_{Switch} the output appears to be V_S chopped into pieces. Play with the frequencies and the scope triggering. Try a case where the switching frequency is much higher than the signal frequency. Make a sketch of the output and comment in your notebook. This is how the "CHOP" mode of analog dual-sweep scope works. It switches its single electron beam back and forth between the two traces very quickly.

Sample and Hold: Most analog-to-digital converters (DAC) require a steady (flat) input voltage while they make the conversion. If the actual input voltage changes a lot, like an audio signal, a special circuit called a "sample-and-hold" is used to take a quick *sample* of the changing voltage and *hold* the input to the DAC flat at that sample voltage while the DAC does its job.

If you place a capacitor across R_L in the circuit above, it becomes a sample-and-hold. Try it with a 0.22 µF capacitor, V_S at 1 kHz, and V_{Switch} at 25 kHz. This combination will show the circuit operation quite well. Notice that the output voltage now appears to be "stepped". The analog-to digital conversion could take place during one of these flat steps. Play with the frequencies and the scope triggering. Make a sketch of the output and comment in your notebook.

MC14069UB