Name: _____ Date:_____ Score:_____/ (75)

This lab MUST be done in your normal lab time— NO LATE LABS

Bring Textbook to Lab. You don't need to use your lab notebook, just fill in the blanks, you'll be graded when you're done.

A. Stolp, 4/17/00
rev,4/19/01

University of Utah
Electrical & Computer Engineering Department
EE 2100
Experiment No. 13

JFET Transistor Introduction

Objectives

1. Measure the characteristics of a junction-field-effect-transistor (JFET).
2. Construct and test a simple amplifier using the JFET.

Check out from stockroom:

- Wire kit
- two 10x probes
- Multimeter

Parts to be supplied by the student:

These items may be bought from stockroom.

- 270, 1 k, 1.5 k, 10 k, 100 k, & two 1 MΩ resistors + others you determine by design
- 0.1 to 1 µF capacitor & two capacitors ≥10 µF
- 2N5486 or 2N5248 JFET transistor (use data for 2N5486 in either case)
- Proto-board and wires

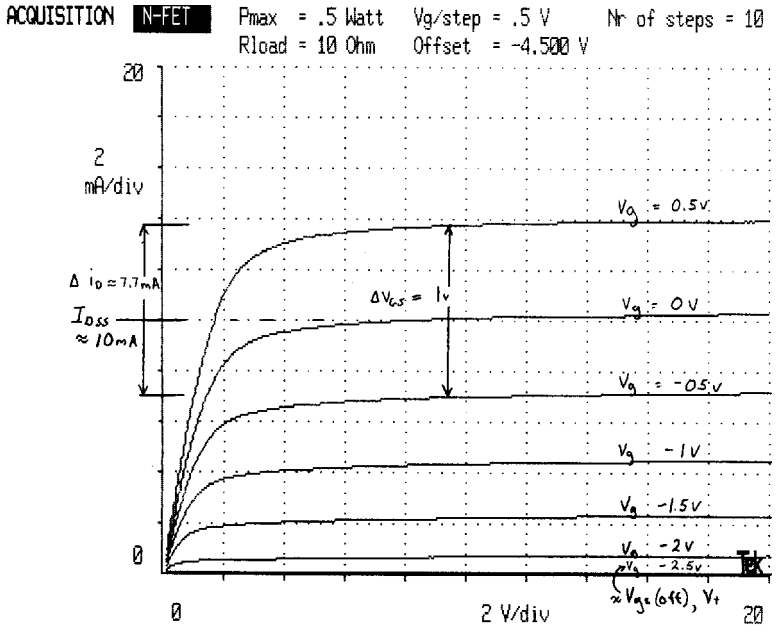
Experiment 1, JFET Characteristics

Data book: Find a transistor data book or a data sheet (may be attached) that covers the 2N5486 JFET transistor. Find the important parameters for this transistor and record them in the blanks or in the table below.

a. Determine the type of transistor (n or p-channel). _____
b. Find the minimum and maximum V_t ($V_{GS(off)}$), and note that the number is negative, confirming that the JFET is a depletion-mode device.
c. Find the minimum and maximum I_{DSS}, which you'll be able to use in calculations.
d. Find the forward transconductance (also called forward transfer admittance) measured with V_{GS} = 0 V (g_{m0}, g_{fs}, or Y_{fs}). I'll refer to this as g_{m0} from now on.

	Data sheet		Curve Tracer	Manual Measurement
	min	max		
V_t				
I_{DSS}				
g_{m0}				

Curve tracer: NOTE: if the curve tracer is in use, skip this step now and come back to it later. Obtain the characteristic drain curves for this FET on the curve tracer (i_D vs v_{DS} for a series of v_{GS} values like those shown at right. Be sure to observe how the FET operates with a small positive gate voltage (<+0.7V) as well as with the more normal negative voltage. When v_{GS} (Vg on curve tracer) is greater than 0V the transistor is operating in the enhancement region. See if the cursor will give you the transconductance (g_m) for the v_{GS} = 0 curve (g_{m0}). Hit the STORE button on the curve tracer. Print a copy of these curves and staple them to the lab. Label the V_{gs} values like I did mine, above.

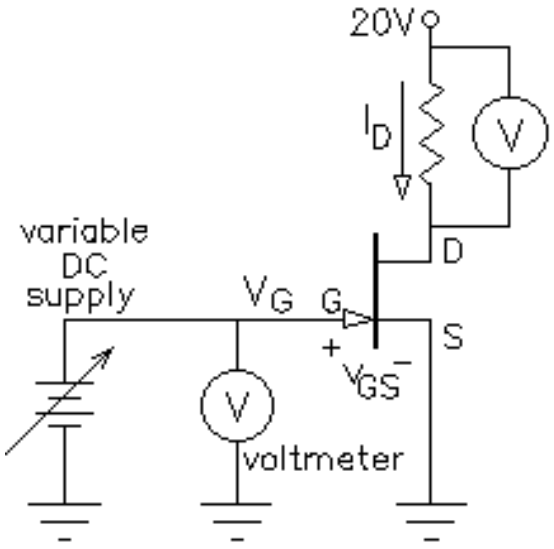


You're going to do something a little strange now, But it should demonstrate just how symmetric an FET is. Pull your JFET out of the connections and put it back in backwards--drain into the S terminal, source into the D terminal and the gate where it should be, in the G terminal. Take a second set of curves over the top of the set you just stored. Are they close to the same?_____ The only difference between the source and drain is that the FET will be designed so that the drain side has better heat dissipation characteristics.

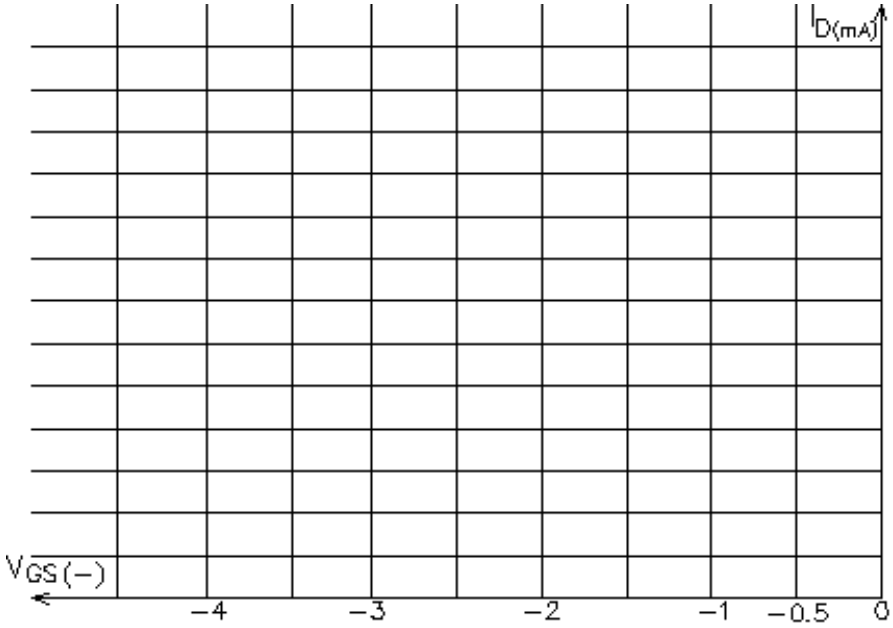
If you were not able to find g_{m0} using the cursor, find it now from your printed curves. Refer to my example curves, above. (on my example curves: $g_{m0} = \Delta i_D/\Delta v_{GS}$ = 7.7mA/1V = 7.7mA/V = 7700 µmho). Find V_t and I_{DSS} for this FET from your printed curves. Note: There is a small chance that your JFET's V_t is less than -4.5V. In that case, you won't be able to find V_t here. Add all these values to the table on the first page.

Manual: Build the circuit shown. This circuit will let you find the V_t ($V_{GS(off)}$) and the transfer characteristic curve (saturation i_D vs v_{GS} like Fig 5.21c, p.378 in your book).

The voltmeter across the 1 kΩ resistor allows you to measure the drain current and the variable voltage supply allows you to vary the gate voltage. Note: You can use two separate outputs of the HP power supply or you can make the HP 33120 output DC by holding down the **Offset** button for 2 seconds. Just remember that it shows double its actual output voltage. ALSO: note the polarity of the DC supply.

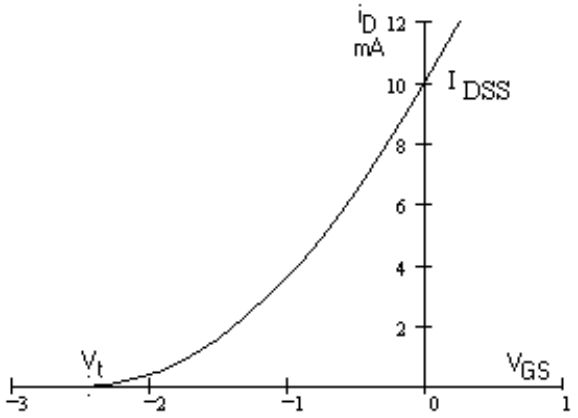


V_{GS}	I_D
0V	



Turn the variable supply down to 0 V, and measure the drain current. Increase (make more negative) the variable supply voltage in small steps and record the data in the table. Take enough points to get a good plot. Pay particular attention to getting a good value for V_t ($V_{GS(off)}$), where $I_D = 0$.

Plot an accurate transfer characteristic curve above. Determine a value for g_{m0} (the slope of the curve at $v_{GS} = 0$,) from your data or plot (draw a tangent line and find its slope).

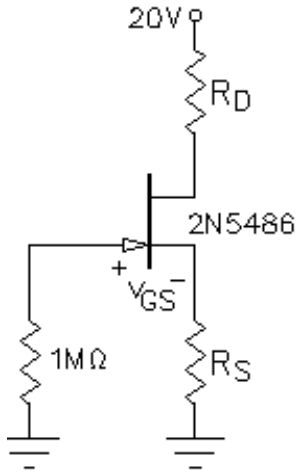


Enter your values of I_{DSS}, V_t, and g_{m0} in the table on the first page. Compare the data-sheet numbers to those you found from the curve tracer and from your measurement circuit.

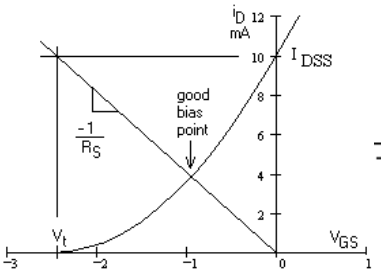
Experiment 2, JFET Amplifier

Bias Design: Figure 2 shows a simple self-bias circuit for a depletion-mode FET. $V_G = 0$ and $V_{GS} = -V_S = -R_s I_D$. Determine a suitable value for R_S from the data sheet numbers. A quick-and-dirty way to find a reasonable R_S is:

$$R_S = \frac{|V_t|}{I_{DSS}}$$



If you look at the curve at right you can see where this comes from. Calculate this once for the maximum $|V_t|$ and I_{DSS} values from the data sheet and once again for the minimum values. Average your two R_S values to pick a standard resistor value for R_S. (Space is provided on the next page.)



$$R_S = \frac{|V_t|}{I_{DSS}}$$ For max $|V_t|$ and I_{DSS} :

For min $|V_t|$ and I_{DSS} :

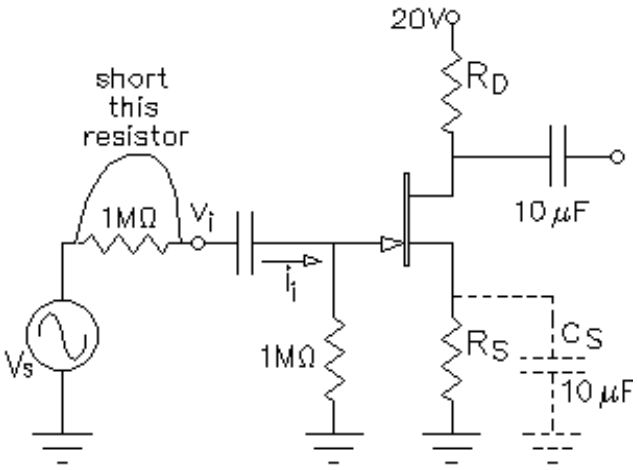
Now that you have a value for R_S, calculate a minimum and a maximum I_D. Solve the equation below for I_D. Do it once for the maximum $|V_t|$ and I_{DSS} values from the data sheet and once again for the minimum values. (I got about 2.9 & 8.1 mA, use those now if you want to make your own calculations later).

$$R_S^2 I_D^2 - 2[(V_G - V_t)R_S + \frac{V_t^2}{2I_{DSS}}]I_D + (V_G - V_t)^2 = 0$$

You'd like to select a value for R_D so that V_D is about midway between V_{DD} and $|V_t|$. Try this for your two cases. Dismal results, aren't they? OK, select R_D so that in the worst case V_D is $|V_t|$ + 2 V (I got about 1.5 kΩ, use that now if you want to make the calculations later). V_D must always be greater than $|V_t|$, no matter what the drain current is, or your JFET will fall out of saturation. (More space on next page.)

Notice that this design process is a pain because the characteristics can vary so much from part to part.

Build amp: Construct the amplifier shown without the bypass capacitor, C_S. Use the values of R_S and R_D that you selected earlier. Measure the DC V_S and V_D and calculate I_D from your measurements. Plot this bias point on your earlier transfer characteristic curve (the one you took manually), it should fall somewhere on the curve.



Gain: Adjust the signal generator to 1 kHz and apply a small input signal and observe both the input and output with the scope. Turn up the input signal until you can begin to see distortion in the output signal. The distortion you are looking for is an asymmetry in the sine wave. Turn the input signal back down to eliminate the distortion. Determine the voltage gain.

How does it compare to R_D/R_S?

Not too close, is it? The gain of an FET amplifier is more difficult to determine than that of a BJT amplifier. It is also generally much lower for a similar circuit.

Add the bypass capacitor, C_S, lower the input and measure the gain again.

Now let' s try something a little strange. In the first step you saw that this FET could also operate with small positive voltages on its gate, in the enhancement region of operation. What if you change the V_{GS} bias voltage to 0 V, that is, short R_S? Think the amplifier will still work? Try it. You may have to turn down the input signal a little to eliminate distortion. What is the new voltage gain?

Why did it go up? (OK, with some FETs it doesn't go up— no, I don't know why, it *should* go up.)

Look back at the transfer characteristic curve you made, and see how the forward transconductance (the slope of the curve) is greater (steeper slope) at this new bias point than at the old one. With this new bias you get the maximum g_m (g_{m0}). Remove the short so R_S is back in the circuit.

Input resistance: Measure the output signal voltage. Remove the short across the 1 MΩ resistor (the one between the signal generator and the input capacitor). Measure the new output signal voltage. Notice how little it changed. What does this tell you about the input resistance of the FET amplifier?

Frequency response: Place the short back across the 1 MΩ resistor or you'll get a lousy frequency response. Turn up the input frequency to find the upper corner frequency (f_{CH}).

Conclusion

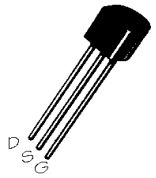
Main Points of the lab

1. The large variability of V_t and the inherent non-linearity of FETs makes it difficult to design a linear amplifier or a circuit with a large output swing. FETs are usually used as small signal amplifiers or switches.
2. FETs don't have very good gain
3. FETs have very high input impedance.

Get your lab instructor to check you off and grade this handout before you tear down your final circuit. No further conclusion is necessary.

2N5484 thru 2N5486

CASE 29-02, STYLE 5
TO-92 (TO-226AA)



JFET
VHF/UHF AMPLIFIER

N-CHANNEL — DEPLETION

Refer to 2N4416 for graphs.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	V_{GSR}	25	Vdc
Drain Current	I_D	30	mAdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = −1.0 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	−25	—	—	Vdc
Gate Reverse Current		I_{GSS}				
(V_{GS} = −20 Vdc, V_{DS} = 0)			—	—	−1.0	nAdc
(V_{GS} = −20 Vdc, V_{DS} = 0, T_A = 100°C)			—	—	−0.2	μAdc
Gate Source Cutoff Voltage		$V_{GS(off)}$				Vdc
(V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5484		−0.3	—	−3.0	
	2N5485		−0.5	—	−4.0	
	2N5486		−2.0	—	−6.0	
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current		I_{DSS}				mAdc
(V_{DS} = 15 Vdc, V_{GS} = 0)	2N5484		1.0	—	5.0	
	2N5485		4.0	—	10	
	2N5486		8.0	—	20	
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance		$\lvert y_{fs} \rvert$				μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5484		3000	—	6000	
	2N5485		3500	—	7000	
	2N5486		4000	—	8000	
Input Admittance		$Re(y_{is})$				μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5484		—	—	100	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5485, 2N5486		—	—	1000	
Output Admittance		$\lvert y_{os} \rvert$				μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5484		—	—	50	
	2N5485		—	—	60	
	2N5486		—	—	75	
Output Conductance		$Re(y_{os})$				μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5484		—	—	75	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5485, 2N5486		—	—	100	
Forward Transconductance		$Re(y_{fs})$				μmhos
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 MHz)	2N5484		2500	—	—	
(V_{DS} = 15 Vdc, V_{GS} = 0, f = 400 MHz)	2N5485		3000	—	—	
	2N5486		3500	—	—	