#### University of Utah **Electrical & Computer Engineering Department** ECE 2100 Experiment No. 10 **Common Emitter with Partial Bypass**

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Minimum required points = 50Recommend parts (all) = 72 points (100%)

# **Objectives**

- 1. Observe the characteristics of a partially bypassed common emitter amplifier as compared to the fully bypassed case you worked with last time.
- 2. Observe the Miller effect.
- 3. See how the load effects the maximum output swing.

# Check out from stockroom:

Wire kit & two 10x scope probes (compensate before using)

## Parts:

51, 27, 270, 820, 1 k, 1.5 k, 3.9 k, 15 k & 56 kΩ, resistors

ΗP

- 0.01  $\mu$ F (probably marked 103), 1 10  $\mu$ F, 10 100  $\mu$ F & 270 470  $\mu$ F capacitors
- 2N3904 transistor

### **Experiment 1, Partially** Bypassed CE amp (29

pts, recomended) Build the common-emitter amplifier shown at right, without the load. This is the almost the same circuit you used in the last lab, and hopefully it's still on your proto-board. The only difference is the 27  $\Omega$ resistor in the emitter circuit.

Notice that from the AC

signals's point of view, the

resistance from the emitter to ground is 27  $\Omega$ ||270  $\Omega$ . This is an what the book calls an emitter degeneration resistance, R<sub>e</sub>.

**Bias:** Check the DC bias voltages (V<sub>B</sub>, V<sub>E</sub>, & V<sub>C</sub>) and make sure that nothing has changed since last time.

Gain: Using the r<sub>e</sub> you found in the last lab (back-calculated from the gain measurement) and neglecting the impedance of C<sub>E</sub>, what signal gain do you expect from this amplifier?



Adjust signal generator amplitude so the output of your circuit is about 4  $V_{pp}$ . Measure the voltage gain ( $A_v = v_{o/}v_{in}$  **NOT**  $v_{o/}v_s$ , the attenuation circuit is NOT part of your amplifier, but is only there because the HP signal generator cannot be turned down far enough). This gain should be significantly lower than in the last lab, but we'll get many improvements in return for the reduced gain.

**Distortion:** Now turn up the input signal as high as you can without causing clipping at the output. Can you see any distortion in the output waveform? Do you see any distortion like you saw in the last lab's fully bypassed circuit? (If you can't remember what the distortion looked like, just short the 27  $\Omega$  resistor and turn the input down to a little less than clipping level. Remove the short when done.) Adjust signal generator amplitude so the output of your circuit is about 4 V<sub>pp</sub> again.

**Input resistance:** Find the Input resistance like you did last week. Refer back to last week's lab handout if you must for detailed information. I described three different ways to find the input resistance. Again, you should use a resistor value about equal to the input resistance you expect to see (3.9 k  $\Omega$  ought to do this time).

Assuming a reasonable  $\beta$ ,  $r_e$ , and  $R_e$ , calculate the expected input resistance and compare. Note: you can make this and most other calculations later, if you want.

Look back at the last lab and find the input resistance of the fully bypassed commonemitter amp. Compare that to what you just found. What did the bypass capacitor do to the input resistance?

**Output resistance:** There is no reason to expect this to be different than last week, so don't bother measuring it again.

**Frequency response:** Compensate a scope probe first and then hook it to the output of your circuit. Vary the input frequency to find the low and high corner frequencies. If you can't find the low corner, mention the lowest frequency that you tried in your notebook. Compare  $f_{CL}$  and  $f_{CH}$  to those you found for the fully bypassed circuit, both the low and high corner frequencies should have improved. Return the input frequency to about 1 kHz.

Calculate the corner frequency due to the input coupling capacitor ( $C_{in}$ ). Calculate the corner frequency due to the emitter bypass capacitor ( $C_E$ ). Compare to your measured  $f_{CL}$  or use your calculations to explain your inability to find  $f_{CL}$ .

Common Emitter Amplifiers			
Parameter	No bypass (R <sub>c</sub> = 820 Ω)	Full bypass	Partial bypass
gain (A <sub>v</sub> )			
distortion			
input resistance (R <sub>in</sub> )	not measured		
low corner freq $(f_{CL})$	not measured		
high corner freq $(f_{CH})$	not measured		

Make a table in your notebook like the one shown.

Fill in your table with measurements that you took in this lab and the two previous labs. You may not have measured data for the full bypass, input resistance entry. In that case use a calculated value and write "(calc)" behind it. Enter subjective comments in the "distortion" row.

You should find from your table that The partially bypassed CE amplifier is a good compromise between the other two circuits.

### Experiment 2, Miller Effect (22 pts, recomended)

Hook a 0.001  $\mu F$  capacitor from the base to ground. Hook a scope probe on the output and vary the input frequency to find the high corner frequency (f<sub>CH</sub>). This should be less than the f<sub>CH</sub> you found just a few minutes ago. If it's not, replace the 0.001  $\mu F$  capacitor

with a larger cap and try again. When you succeed in making  $f_{CH}$  lower than it was, then your new capacitor is creating the dominant high frequency pole.

Now move the capacitor so it's hooked from the base to the collector. Find the new high corner frequency ( $f_{CH}$ ). This should be way less than what you just measured. In fact, the first  $f_{CH}$  should be about  $(A_v+1)$  times higher than this one (where  $A_v$  is the voltage gain of this amplifier). Any idea why? Think about this. The capacitor was originally hooked to ground. The voltage across the capacitor was  $v_{\rm h}$ . Now the capacitor is hooked to the collector, where the signal voltage is A<sub>v</sub> times bigger and inverted as well. The voltage across the capacitor is now  $(A_{v+1})$  times bigger and the signal current through it is also  $(A_{v+1})$  times bigger. That means that a capacitor hooked from the base to the collector is equivalent to an  $(A_v+1)$  times bigger capacitor hooked from the base to ground (at least from the base's point-of-view). Either capacitor would have the lowered  $f_{CH}$  in the same way. That's the Miller effect— a capacitor hooked between the input and output of an inverting amplifier affects the



frequency response in the same way as one  $(A_v+1)$  times bigger hooked between the input to ground. Capacitance between the base an the collector has an exaggerated effect on the frequency response of the amplifier.

In truth, you would almost never hook a capacitor where you have one hooked now. That would be dumb. But, because the collector-base junction in the transistor acts like a capacitor, we don't have to be dumb, the transistor will be dumb for us. Because of the Miller effect, The  $C_{CB}$  capacitor inside the transistor will usually limit the high frequency response of the amplifier.

Compare your two  $f_{CH}$  frequencies and see if they are indeed about a factor of  $(A_v+1)$  times apart. Comment on the Miller effect in your notebook. Remove your extra capacitor and turn the input frequency back down.

Now lets take a look at a very practical way to use your new knowledge of the miller effect. The proto board that you use to make circuits in the lab has a considerable capacitance between adjacent rows of connections Your transistor is almost certainly inserted into the proto board so that the base an collector are in adjacent rows– that means extra capacitance between the base and collector and consequently a lower  $f_{CH}$  than necessary. If we could get the base lead further from the collector then maybe our frequency response will go up-- worth a try... Pull your transistor out and bend the



collector lead over a little so that it will fit into the next row over (one row further away from the base). Now put it back in the proto board and move the other collector connections over to the new row. Hook the row between the base and collector to ground to help shield the base from the collector. Find the new  $f_{CH}$  and compare it to what you got last time. When I tried this my  $f_{CH}$  went up by about 1 MHZ. These sorts of tricks are routinely used in PC board layouts. Comment in lab notebook.

# Experiment 3, Effects of the load (21 pts, recomended)

**Clipping without load:** Hook a scope probe to the collector ( $v_c$ ). Set the scope to 2 V/div, DC coupling, and adjust the position until ground is at the bottom of the screen. This way you'll be able to see both the DC and the AC voltage of the collector voltage at the same time. Adjust signal generator amplitude so the output of your circuit shows no clipping or distortion. Measure the DC average voltage V<sub>c</sub>. Turn up the input signal level until the output begins to clip. Does it clip first at the top, or at the bottom of the waveform? Turn down the input just enough to eliminate the clipping. What is the maximum unclipped output ( $V_{oppmax}$ )? Turn the input level back down again. Calculate the expected  $V_{oppmax}$  and compare to what you found (use equations below without R<sub>I</sub>).

Positive clipping limit:  $L^+ = I_C r_c$  and negative limit:  $L^- = (V_{CE} - 0.5V) \frac{r_c}{r_c + R_e}$ 

where  $r_c = R_c || R_L$  and  $R_e = R_E || 27\Omega$ 

 $V_{\text{oppmax}}$  is 2L+ or 2L-, whichever is smaller. Notice that I used  $V_{\text{CE}}$  - 0.5V rather than  $V_{\text{CE}}$  - 0.2V. This reflects the fact that although  $V_{\text{CE}} \approx 0.2V$  in "hard" saturation, you will often begin to see the effects at  $V_{\text{CE}} \approx 0.5V$  or even higher.

**Effects of the load:** Add a 1 k $\Omega$  load resistor (R<sub>L</sub>). Measure the signal voltage gain (A<sub>v</sub> = v<sub>c</sub>/v<sub>in</sub>). Why is it lower than was without the load? Calculate the expected gain and compare to what you found.

Turn up the input signal level and find the maximum unclipped output ( $V_{oppmax}$ ). How does this compare to what you found without the load? Turn the input level back down again. Calculate the expected ( $V_{oppmax}$ ) and compare to what you found.

#### Main points:

- 1) A partially bypassed circuit has less distortion, higher Input impedance and better frequency response than the fully bypassed, but at the cost of some gain.
- 2) Capacitance between the input and output of an inverting amplifier appears to be  $(A_v+1)$  times bigger than it actually is.
- 3) The gain and the maximum output voltage swing are both adversely affected by the load.