Implementation of a Cognitive Radio Modem
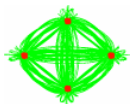
P. Amini, E. Azarnasab, S. Akoum,

X. Mao, H. Rao, B. Farhang-Boroujeny

Outline

1) **Problem Statement**
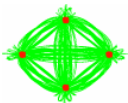
   $\rightarrow$ **Spectrum Access for First Responders**

   $\rightarrow$ **Hardware Platform**

2) **Spectrum Sensing**

3) **Transceiver and MAC Layer**

4) **Hardware Implementation**
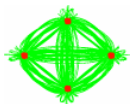
5) **Results**

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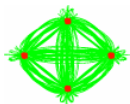**THE UNIVERSITY OF UTAH**

Problem Statement

- **Disaster Scenario**: first responders should have the ability to communicate and exchange information.

- **Scarcity of available spectrum:** is the greatest obstacle for wireless networks.

- **Cognitive Radio**: is a possible solution to the spectrum access obstacle.

- **First Responders:** can use idle portions of the spectrum to communicate with each other.
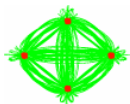
Hardware Platform

- Small Form Factor (SFF) SDR platform: Lyrtech, TI, and Xilinx

- RF-to-baseband platform

- TMS320DM6446 system-on-chip

  - C64x+DSP core, 594 MHz

  - ARM926 core, 297 MHz

- Virtex-4 SX35 FPGA

- RF module operating between 360 and 960 MHz

- Selection of bandwidth (5 MHz or 20 MHz)

Problem Summary

- Family Radio Service (FRS): 462-467MHz band used to implement the cognitive radio network to transmit voice and data.

- 200 Subcarriers of each 25 kHz Bandwidth are used for data and voice transmission

- Challenges:
  - Awareness: Nodes must be able to *sense* the channel for primary licensed users.
  - Coexistence: Share information with other cognitive nodes, communicate reliably and avoid legacy devices.

Outline

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Spectrum Sensing

- Secondary Users (SUs): need to dynamically and reliably determine the spectrum holes.

- Existing solutions:
  - FFT/OFDM: has been proposed as a spectrum sensing as well as communication method suffers from large side lobes, i.e., significant spectrum leakage.
  - Multi-taper method: Computationally expensive.

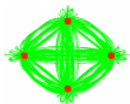- Filterbanks: used for spectrum sensing.
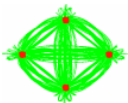
Spectrum Sensing

Superior performance: in terms of the spectral dynamic range when compared with the FFT techniques.
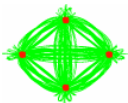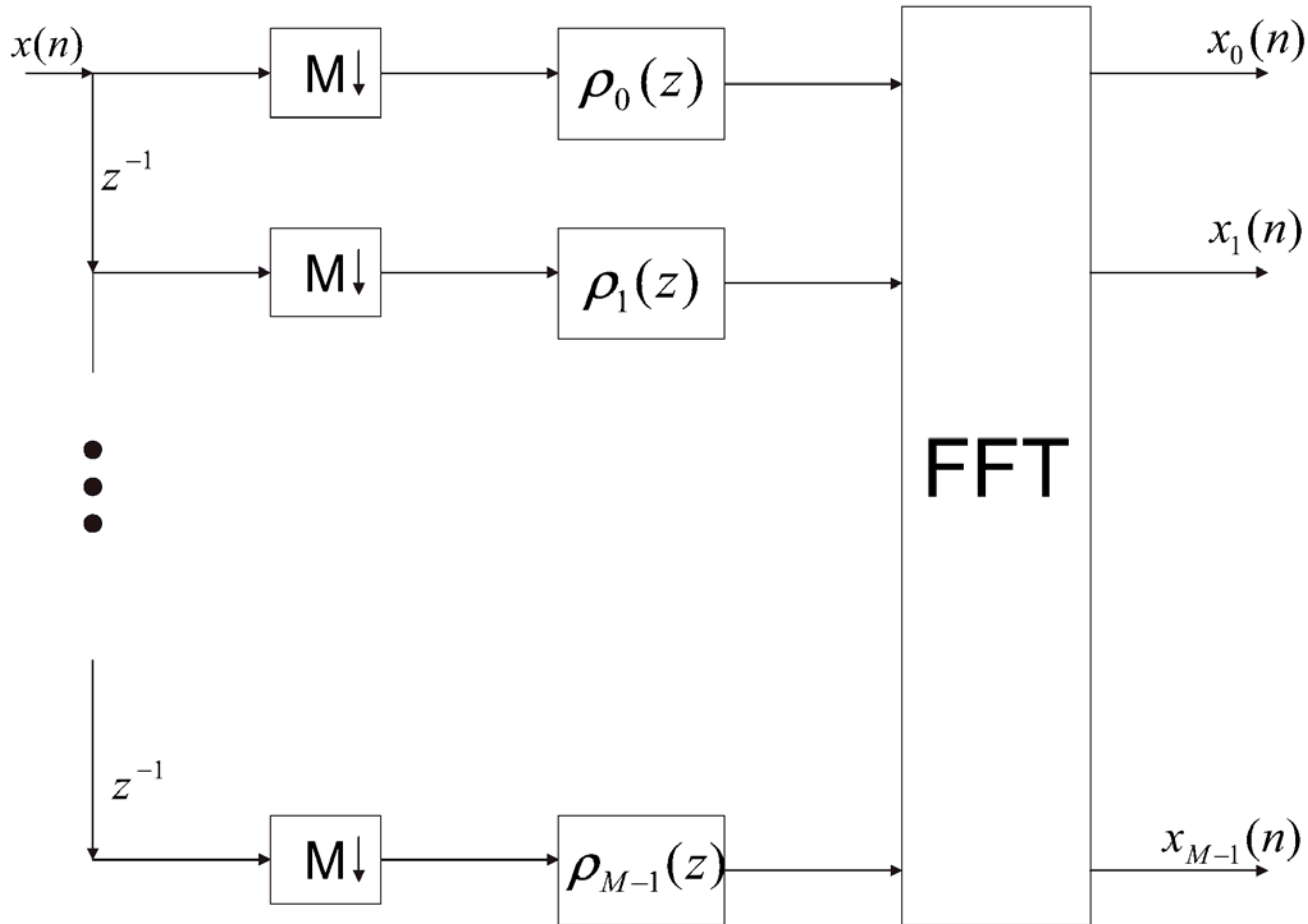
High spectral dynamic range: enables reliable detection of low power users.

> Side lobes of each sub-carrier can be made arbitrary small, hence reduces spectral leakage and improves the spectral dynamic range.

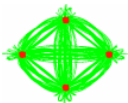Distributed sensing method: used to ensure reliability.
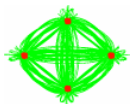
Polyphase Implementation of Filterbanks

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Transmitter

- Software defined modem provides 2 types of services:
  - 19.2 kbps computer-to-computer data stream.
  - 16 kbps Continuously Variable Slope Delta Modulation (CVSD) vocoded voice.
- Channel Coding
  - Data: rate 1/2, constraint length 7, Convolution encoder
  - Voice: Reed-Solomon that correct up to 6 bytes
- Symbol Mapping:
  - Data: QPSK
  - Voice: 8 PSK
- The rest of the modules are the same for voice and data

- Packet Length: 2048 Symbols

- Upconversion is done using a combination of:
  - Cascaded-Integrated-Comb (CIC) filters, and
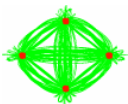 - A novel combined pulse-shaping and CIC compensation filter having the Nyquist-M property.

> The combination of CIC and PSF filters achieves less passband ripple, more stopband attenuation and less ISI when compared with other existing techniques.

- The combined filter takes less space in the FPGA

- Modulation: upconverted signal is modulated to IF for transmission over the channel.

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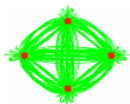
Receiver

- Synchronization: is performed using a *cyclic preamble*

- Cyclic preamble: generated using 3 BPSK modulated pseudo random sequences, each having length 64.

- Why do we use a cyclic preamble?
  - Repetition structure allows us to detect the packet using autocorrelation.
  - Estimate phase and carrier offsets.
  - Enables equalizing the channel effects when coupled with a fractionally spaced cyclic equalizer.
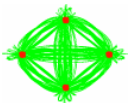 - Exhibits good performance and is easy to implement.

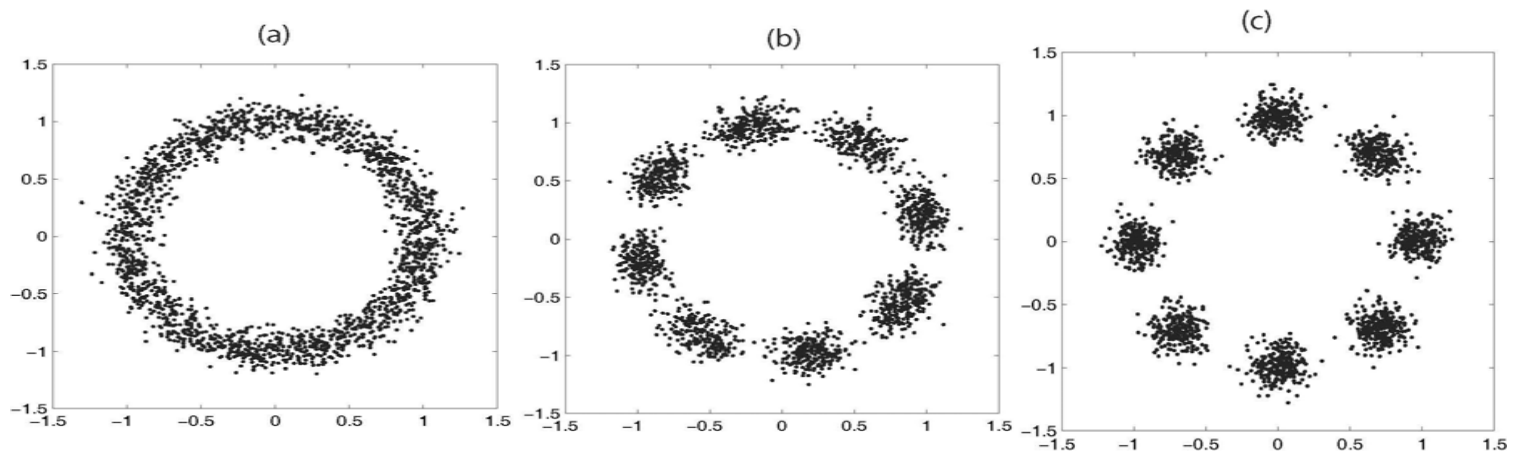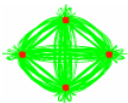## Receiver Structures
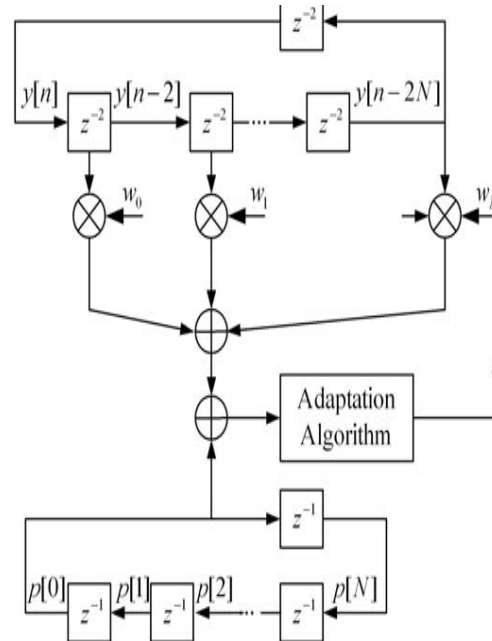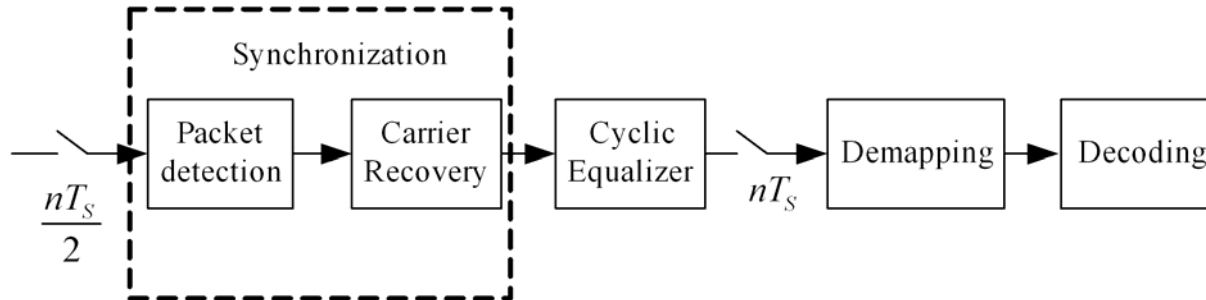
Cyclic Equalizer

Eye Diagrams

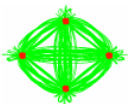

The received signal after
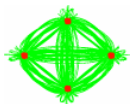(a) packet detection (b) carrier recovery (c) equalization
SNR = 9dB.

MAC Layer Key Features

- Base Station Centric: with uplink and downlink Control Channel(s)

- FDD: SUs use frequency-division duplexing (FDD) to communicate with each other.

- FDMA: The medium access method is frequency-division multiple access (FDMA).

- Coexistence: is the primary goal.

MAC Layer

- Control Channels: are used for coordinating sensing information, controlling leaf node communications, and other management tasks.

- Channel Sensing: each leaf node stops transmitting and senses the entire channel periodically.

- Transmitting Sensing Information: leaf nodes transmit to the base-station if the channel status changes.

MAC Layer

- **Compiling Sensing Information:** The base station receives and compiles the channel state data from all the leaf nodes and itself.

- **Broadcasting Sensing Information:** The base station broadcasts the channel allocation table to all the leaf nodes.

- **The number of uplink control channel(s)** is proportional to the number of leafnodes.
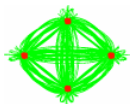
Outline
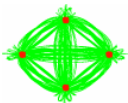
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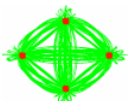
Hardware Layout

- **Processing:**
  - TMS320DM6446 Digital Media Processor (DMP) System on Chip
  - Virtex-IV XC4VX35 FPGA

- **ARM9** is mainly used for INTEGRITY RTOS and overall system control

- **Data conversion module:**
  - 125 MSPS,14-bit dual channel ADC
  - 500 MSPS 16-bit dual channel DAC

- **RF-module** modulate\demodulate the signal from/to RF to/from IF at 30MHz

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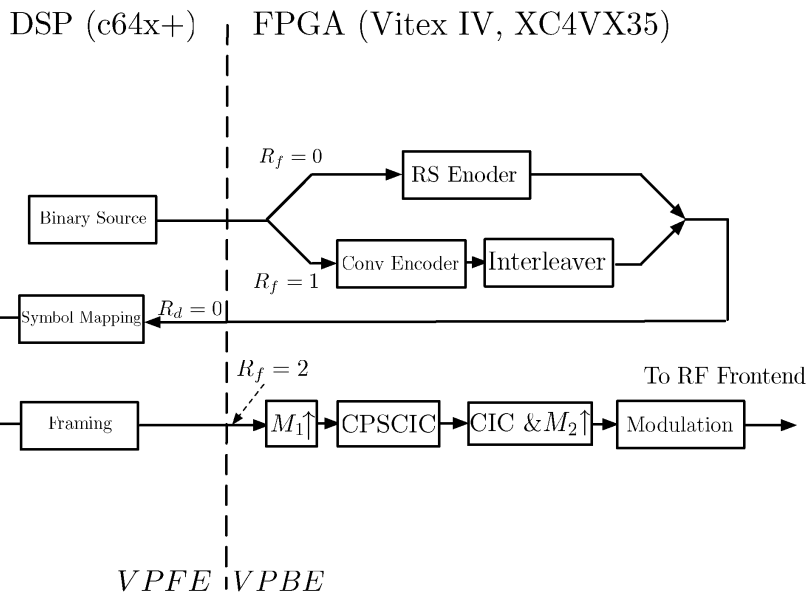**THE UNIVERSITY OF UTAH**

Hardware Layout

- Tasks are divided between DSP core and the FPGA.

- The division of was made based on:
  - the availability of computational resources
  - the extra functionalities offered by TI and Xilinx:
    - Xilinx Logicore Blocksets for FPGA
    - Optimized DSP libraries written for C64x+ core.
- Video Processing Sub-system (VPSS) is DM6446 DSP 16-bit synchronous video transfer port

- VPSS and a shared memory of 8 32 bits registers are used to transfer data to and from the DSP.
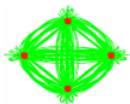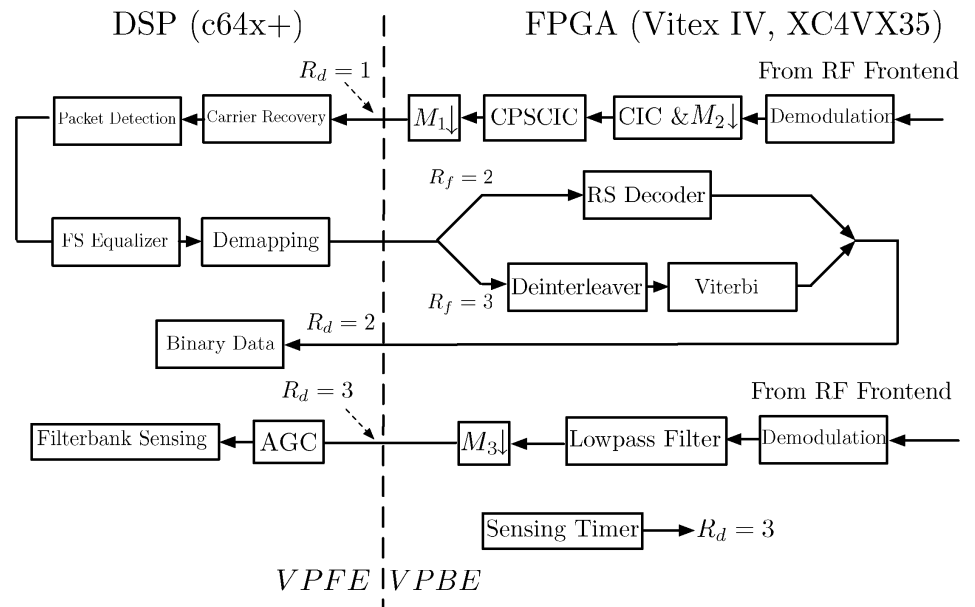
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(a) Transmitter

(b) Receiver

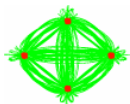DSP (c64x+)   FPGA (Vitex IV, XC4VX35)

DSP (c64x+)   FPGA (Vitex IV, XC4VX35)
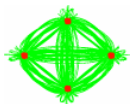
DSP Development

- A complete Simulation was Developed in MATLAB and Simulink

- Some blocks were developed using Real Time Workshop (RTW) while the rest was simulated in Simulink

- Target Language Compiler (TLC) was used to develop the blocks

- Real Time Workshop
  - Fast prototyping
  - can not full fill the real time and memory requirement

DSP

- A Hardware in the Loop (HIL) technique was developed that interfaces MATLAB with the board

- C Code was developed in TI Code Composer Studio

- Modules are moved to the board while the rest are Simulated in MATLAB

- TI CCS is used to combine the RTW code with the rest of system

FPGA
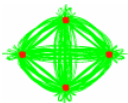
- Xilinx System Generator is used to Develop most of the modules

- Simulink is used to test and simulate the developed modules.

- The generated HDL satisfies the real time requirement of our system

MAC Layer Development

- The MAC layer functionalities simulated using Discrete Event System Specification (DEVS) package in Java

- Java is interfaced to MATLAB and the hardware.

- The PU traffic is emulated using a Vector Functional generator

- MAC functionality is gradually migrated to hardware
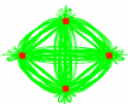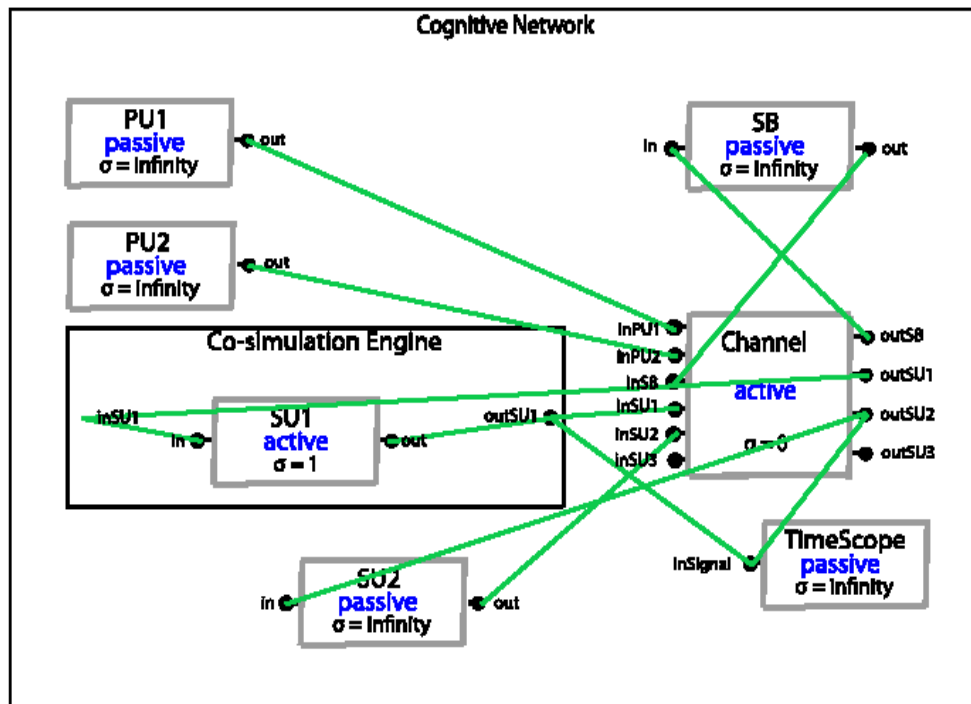
Outline

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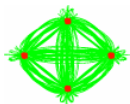
Results: Sensing

- Filterbank: Performed in DSP
- FFT and FFT with hanning: performed on the received signal in MATLAB
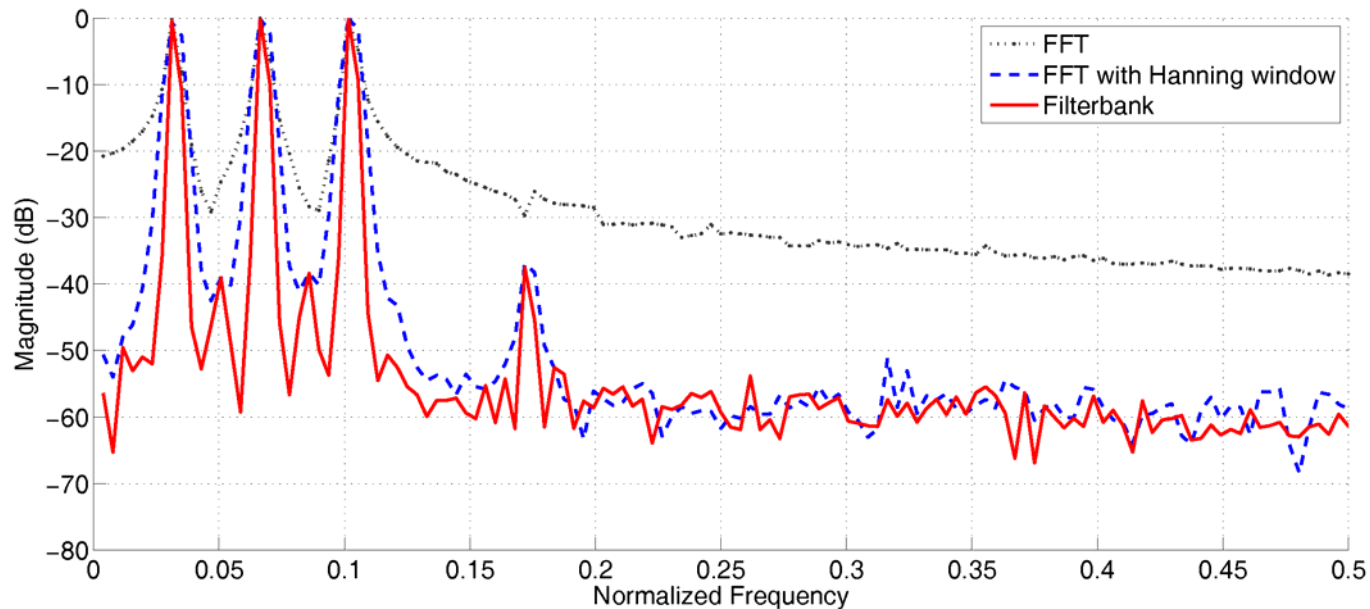
Results: Cognition and Voice transmission

- Using an arbitrary signal generator, the interference of primary users over 5 MHz of bandwidth is emulated.

- We are able to show that our cognitive node can move to an unoccupied frequency band when a primary user starts transmitting on the carrier that is currently in use.

- We transmit voice between two SFF SDRs to show that our cognition works.

Channel

PSD axis: 0, -5, -10, -15, -20, -25, -30, -35, -40, -45, -50, -55, -60, -65, -70, -75, -80, -85, -90, -95

f axis: 25, 50, 75, 100, 125, 150, 175, 200, 225, 250

Legend: — Filterbank — FFT — FFT with Hanning

Left panel controls:

se
- ☑ Filterbank
- ☑ FFT
- ☑ FFT with Hanning
- ☑ Realime Sensing

Sense Once

nsceiver

Transmitter Connect

Receiver Connect

oad

sing

Reload DSP Sensing

Reload FPGA Sensing

nsmitter

Reload DSP Transmitter

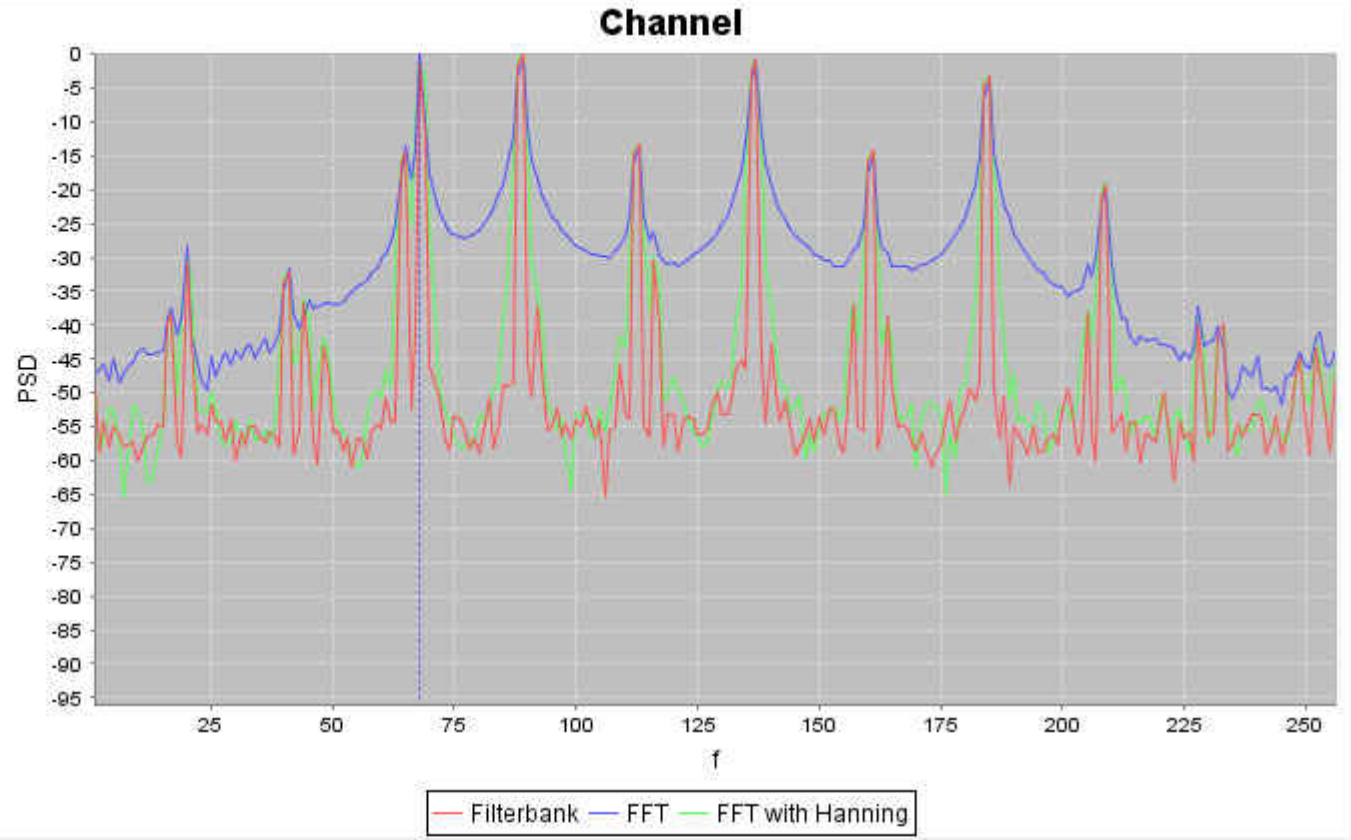Reload FPGA Transmitter

eiver

Reload DSP Receiver

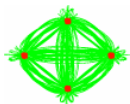Reload FPGA Receiver

Threshold (0 to 96)

40

Set Threshold

Events

Connecting to transmitter SFF SDR board
Successful Connection to Trnasmitter board : ac30048
FPGA loaded to transmitter c:\boz\fpga_trns_cw.bit
DSP loaded to transmitter c:\boz\Trans.out
Transmitter changed to DDS : 205437010 Carrier : 19
Receiver tuned to 205437010
Connecting to sensing SFF SDR board
Successful Connection to Sensing board : a4b008
FPGA loaded to sensing c:\boz\sense1_cw.bit
DSP loaded to sensing c:\boz\Sense.out
DSP loaded to receiver c:\boz\Rec.out
DSP loaded to sensing c:\boz\Sense.out
DSP loaded to sensing c:\boz\Sense.out
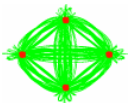DSP loaded to sensing c:\boz\Sense.out

Hardware Demo

Future work

- Combining all the developed modules to complete the transceiver functionality

- Develop MAC Layer Functionality over ARM9 Core using Greenhills MULTI

- Use FLUX group testbed to act as primary users
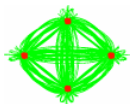
Acknowledgment

We would like to thank the **hardware and software support** that we have received from

- SDR Forum
- Lyrtech
- Texas Instruments
- Xilinx
- Mathworks
- Greenhills
- Prismtech
- Zeligsoft
- Synplicity

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Questions are welcome!

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