SPECTRUM ACCESS FOR FIRST RESPONDERS: IMPLEMENTATION

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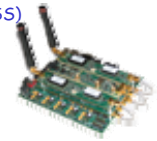
Architecture Platform

SFF SDR platform: provided by Lyrtech and Texas Instruments
Division of tasks: signal processing functions divided between the FPGA and the DSP, ARM9 used for overall system control

Video Processing Sub-system (VPSS) and custom registers are used to interface DSP and FPGA.



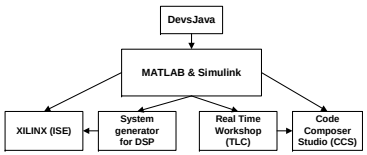
Development Tools

Simulink: used to simulate a working transceiver system before implementation.
Sysgen for DSP: Xilinx add-on to Simulink, used to create the FPGA blocks in collaboration with Xilinx ISE.
RealTime Workshop (RTW): used only for rapid prototyping & testing.
Code Composer Studio (CCS): used to generate the code of the complete DSP subsystem.

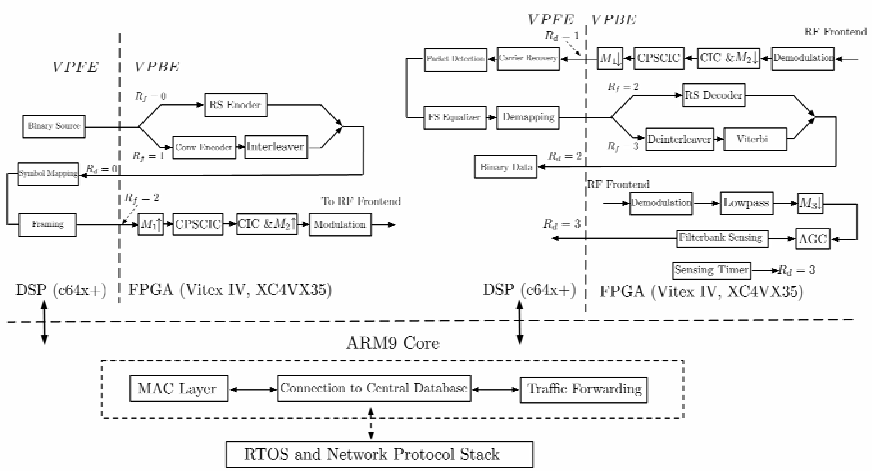
Hardware in the loop technique (HIL): developed by the team:
HIL using MATLAB
HIL using MATLAB and Discrete Event System Specification (DEVS) Java

Development Methodology

Simulink & RTW: used for development and testing of some individual modules and subsystems.
MATLAB and novel HIL interface: used for system integration, optimization and final implementation.
DEVSJava MATLAB Combination: used for developing networking functionality



Transmitter / Receiver



Transceiver Implementation

Modules developed and tested on the hardware include:

- ✓ Timing & Carrier Recovery in DSP
- ✓ Combined Pulse Shaper and CIC (CPSCIC) in FPGA
- ✓ Packet detection in DSP
- ✓ Symbol Mapping/Demapping in DSP
- ✓ Channel Coding in FPGA
- ✓ CVSD Voice Codec in DSP

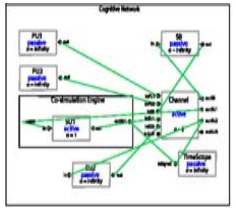
Cognition system Implementation

- ✓ Incoming sensing information demodulated in FPGA using DDS centered at the IF frequency.
- ✓ Demodulated signal downsampled and filtered in FPGA
- ✓ Filterbank Sensing method implemented in DSP.
- ✓ Sensing activated periodically
- ✓ Transmission is halted while sensing is performed.
- ✓ The spectrum is time tagged and weighted to find a suitable band to transmit on.

Mac co-simulation: DevsJava & MATLAB

HIL co-simulation using emulated PUs and SFFSDR platform to model the SUs.

Primary Users (PUs): An Agilent ESG signal Generator used to Generate PU traffic.



Hardware Demo: Sensing

- ✓ A complete simulation is performed first in MATLAB.

Spectrum sensing is presented using the developed MATLAB HIL technique.

- ✓ ESG signal generator is then used to emulate PU traffic.
- ✓ Real time Filterbank sensing is performed on the board
- ✓ FFT & FFT with Hanning window are performed in MATLAB
- ✓ The results are presented using MATLAB

Hardware Demo: Cognition

- ✓ Voice is transmitted between two boards
- ✓ The Tx board performs sensing and transmission.
- ✓ The cognitive radio switches to an unoccupied band when it detects interference on its carrier.
- ✓ The interface to the board is developed using Java and MATLAB compiler for Java
- ✓ A third board is used to sense, the results are reported in Java for demonstration purposes.

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