ECE 5320-- Grounding

References: High Speed Digital Design, by H. Johnson,
Chapter 5 (pp. 189-221)
Homework: read this section

Grounding:

Return Current – Source current passes from +V to ground. Return current passes along the ground back to the source.

Low Frequency Return Current : follows path of least resistance ... distributes over whole ground plane.
High Frequency Return Current: follows path of least inductance .... stays tightly bunched under traces.

Viewgraph FIGURES 5.1 and 5.2

Ground Plane Options:

1) Solid (always the best grounding, but it takes up a WHOLE side of a circuit board)
2) Individual Lines (not as good grounding, but can be optimized to do the best it can)
   (a) Cross hatch (pretty good)
   (b) Fingers (bad)
   (c) Use of Guard traces (almost as good as solid ground, but take room on top of ckt board)

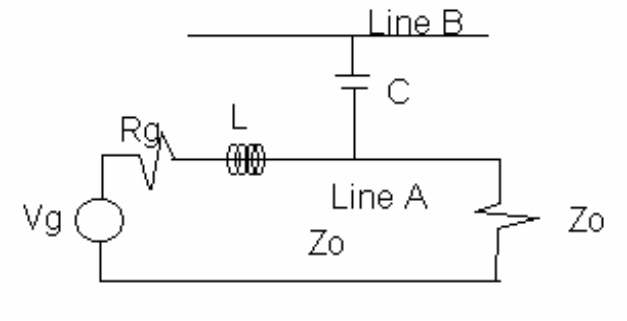
Viewgraphs FIGURES 5.10, 11,13

Solid Ground Plane:

- Best grounding you can do in single-layer board.
- In multi-layer board, solid ground planes may be used for physical strength. Make as many connections between ground planes as you can afford.

Problems encountered in Solid Ground Plane:

1) Slots: Viewgraph Figure 5.8
   - Slots are often used to allow routing of an additional trace as needed.
   - Even for very, very thin slots, current must pass AROUND slot. This increases inductance, and slows down rising edges of pulses.
   - Inductance L = 5 D ln (D/W) (where D = slot length, W = width of trace)
   - If trace is at end of slot instead of middle, inductance is less.
   - Rise Time: (found from series L-R(Zo) "filter")
     T (10-90 percent) = 2.2 L / 2 Zo
   - Cross talk: Another line is close to the first, and creates a capacitive load. We now have an RLC network:



- This network may oscillate:
  $Q = (L/C)^{1/2} / Rg$ If $Q > 1$, circuit rings. If $Q < 1$ circuit rise time is slower than expected. If $Q = 1$, circuit rise time $T(10\text{-}90\ \%) = 3.4\ (LC)^{1/2}$

Connector Pins:
When connectors are attached to ground plane, pins are used. If the holes for these pins are drilled too large or too close together, they remove the current path, create a current loop, and act like a slot.

Cross – Hatched Ground Planes:

Viewgraph FIGURE 5.10

- Cross hatched ground plane is second best to solid ground plane.
- Currents will follow ground traces adjacent to signal wires.
- Capacitors at power-ground crossovers must be GOOD.
- Traditional capacitors will have so much lead inductance that they cannot be used at high frequencies.
- If you can only use two layers, this method MAY work, but probably won't for high speed logic.

Ground Fingers:
Viewgraph Figure 5.11

- Method NOT suitable for high speed design
- Current must flow all the way back to central location.
- Large inductance.

Guard Traces:
Viewgraph FIGURES 5.12,13,14

- Guard trace fits where S = 3W
- Can reduce cross talk by factor of 10.

Multilayer Boards:

Viewgraph FIGURE 5.24,25,26

- Ground Planes connected by vias (be sure holes do not overlap)
- Use solid ground planes to isolate signal layers. Solid ground planes also give rigidity.
- Use many vias to connect planes (reduce signal path of return currents)
- Keep ground planes and power next to eachother.

FCC Regulations Concerning Radiated Noise:

- Problem-makers:
  - Capacitors with currents passing through them get voltages across them and radiate. Avoid bypass capacitors.
  - Cross talk is also coupling with the external environment ... If you can have cross talk, you can also have radiation.
  - Packaging should shield from outside. Everyplace that power passes into shielded package creates strong (concentrated) currents. Most radiation comes from these "holes".

Ground Bounce:

(Text section 2.4.1)

Viewgraph FIGURE 2.16

1) Switch B closes.
2) Current discharges through capacitor and inductor Lgnd.
3) Vgnd = Lgnd dI / dt
   Circuit's ground is no longer "ground". Depends on speed of discharge

Double Clocking:
Viewgraph Figure 2.17

Magnitude of Ground Bounce:

$|Vgnd| = (L \Delta V / T_{10\text{-}90}) / R$

Methods to Reduce Ground Bounce:

- Reduce Lead Inductance (Viewgraph FIGURE 2.20, Table 2.3)
- Slow Down Output Switching Time
- Multiple Ground Wires (BE SURE each has a separate path to ground, not connected together to the same trace then to ground.)
- Ground Wires evenly spaced.
- Provide extra path, directly to external ground, for any differential comparators.