Ground Planes and Layer Stacking

POINTS TO REMEMBER:

For printed circuit board traces, the most critical dimension is the ratio of trace width to height above ground.

Double the reflection budget to find the allowed mismatch between the characteristic impedance and the terminating resistors.

Large variations in physical dimensions make a small impact on the resulting impedance.

The slope of any function plotted on log-log paper is equal to the sensitivity of the function to changes in its argument.

All formulas for transmission velocity are inversely proportional to the effective square root of electric permittivity.

Ground and power planes in high-speed digital systems perform three critical functions:

- Provide stable reference voltages for exchanging digital signals
- Distribute power to all logic devices
- Control crosstalk between signals

This chapter focuses on signal crosstalk. Sections 5.1–5.5 assume relatively short traces, for which a lumped analysis of mutual inductance is appropriate. Section 5.7 treats the case of long lines, where we separate coupling into forward and reverse parts.

Section 5.8 summarizes the rules for designing good printed circuit board layer stacks that control crosstalk.

The formulas in this chapter are accurate only to within a factor of 2. For better accuracy use the formulas as a guide and build a prototype, and then measure its actual performance. Many transmission line structures are easily built out of copper tape and blank circuit board material.

The formulas in this chapter are excellent for showing how electromagnetic effects adjust in response to physical changes. For example, if crosstalk is 30% too high, the formulas can show just how much further to separate your traces. They are less useful for predicting the absolute value of any particular effect.

5.1 HIGH-SPEED CURRENT FOLLOWS THE PATH OF LEAST INDUCTANCE

At low speeds, current follows the path of least resistance. In reference to Figure 5.1, low-speed current transmitted from A to 3 returns to the driver along the ground plane. This return current flows in wide arcs on its way back to the driver. The current density along each arc corresponds to the conductance of that path.

*L*Sometimes reported as plating weight. Each ounce of plating weight is 0.00135 in. thick.
At high speeds, the inductance of a given return-current path is far more significant than its resistance. High-speed return current follows the path of least inductance, not the path of least resistance.

The lowest inductance return path lies directly under a signal conductor, minimizing the total loop area between the outgoing and returning current paths. Returning signal currents tend to follow this direct path, close underneath the signal conductor. Figure 5.2 shows a typical high-frequency return-current path.

Figure 5.3 presents the cross section of a typical printed circuit board trace along with its return-current distribution. The peak current density lies directly under the trace. The current density then falls off sharply to each side.

An approximate relation for the return-current density at a point \( D \) inches away from a signal trace is

\[
i(D) = \frac{I_0}{\pi H} \frac{1}{1 + (D/H)^2}
\]

[5.1]

\[\text{where } I_0 = \text{total signal current, A} \]
\[H = \text{height of trace above circuit board, in.} \]
\[D = \text{perpendicular distance from signal trace, in.} \]
\[i(D) = \text{signal current density, A/in.} \]

Current density at point \( D \) is proportional to

\[
\frac{1}{1 + \left(\frac{D}{H}\right)^2}
\]

Figure 5.3 Distribution of high-frequency current density underneath a signal trace.

The current distribution (Equation 5.1) balances opposing forces. Were the current more tightly drawn together, it would have higher inductance (a skinny wire has more inductance than a broad, flat one). Were the current spread farther apart from the signal trace, the total loop area between the outgoing and returning signal paths would increase, raising the inductance (inductance is proportional to loop area). Equation 5.1 specifies the optimum distribution minimizing the total loop inductance of both outgoing and returning current paths.

The current distribution (Equation 5.1) also minimizes the total energy stored in the magnetic field surrounding the signal wire.

**POINTS TO REMEMBER:**

1. High-speed current follows the path of least inductance.
2. Returning signal currents tend to stay near their signal conductors, falling off in intensity with the square of increasing distance.

### 5.2 CROSSTALK IN SOLID GROUND PLANES

Crosstalk between two conductors depends on their mutual inductance and their mutual capacitance. Usually, in digital problems the inductive crosstalk is as big or larger than capacitive crosstalk, so we will henceforth discuss mainly the inductive coupling mechanism.
The theory behind mutual inductive coupling for lumped circuits appears in Section 1.10. That theory postulates that returning signal currents will generate magnetic fields. Those magnetic fields in turn induce voltages in other circuit traces.

The induced voltages are proportional to the derivative of the driving signal. They become markedly worse as rise times get shorter.

Because the returning current density and its associated local magnetic field strength drop off according to Equation 5.1, we suspect that mutual inductive crosstalk also drops off as we move the two traces in Figure 5.4 away from each other.

\[
\text{Crosstalk} = \frac{K}{1 + (D/H)^2}
\]  \hspace{1cm} (5.2)

![Figure 5.4 Cross section of two traces showing crosstalk.](image)

Here we are expressing crosstalk as a ratio of measured noise voltage to the driving step size. The constant \( K \) depends on the circuit rise time and the length of the interfering traces. \( L \) is always less than 1.

We can check this hypothesis with a simple experiment. The traces configured in Figure 5.5 are 26 in. long and separated by 0.080 in. center to center. They lie on a single-layer main circuit board. The ground plane for this experiment is a solid copper sheet fastened below the main circuit board. Together, the main board and the ground layer sandwich a pile of dielectric spacers of known thickness. By this arrangement we can simultaneously vary the effective height above ground of the driven and receiving traces.

As in problems involving characteristic impedance, the ratio of sizes is more important than the absolute dimensions. In this case, it is the ratio \( D/H \) that determines the crosstalk. By varying the trace height above ground, we can control the ratio \( D/H \).

Figure 5.6 plots the resulting step responses, measured at point \( D \), when driving the input with a 35-V step. Figure 5.6 sees ground separations of 0.010, 0.020, 0.030, 0.040, and 0.050 in. The last race (biggest noise pulse) was taken with no ground plane at all.

Figure 5.7 compiles this measured data into a chart showing the mutual inductance between traces as a function of the ratio \( D/H \). Area is used as a measure of mutual coupling, as explained in Section 1.8. By measuring the area we can factor out the tendency.
of the driving waveform to slow down when confronted with a high loop inductance. This effect shows in the resulting noise plot as a lengthening of the noise pulse at high coupling factors.

**Points to Remember:**

- Returning signal currents generate magnetic fields, which in turn induce voltages in other circuit traces.
- The induced noise coupled into adjacent traces falls off with the square of increasing distance.

**Crosstalk in Slotted Ground Planes**

The crosstalk situation depicted in Figure 5.8 is a classic layout mistake called a **ground slot**.

Ground slots happen when a layout engineer runs out of room on the regular routing layers and decides to cram in a trace on the ground plane layer. This is done by cutting a long slot in the ground plane and laying the trace in the slot. Ground slots add inductance to traces passing perpendicularly over the slot, and increase crosstalk. Do not tolerate this practice.

Ground slots also happen on dense backplanes which pass through fields of connector pins. Always make sure the ground clear-outs around each pin have ground continuity between all pins (Figure 5.9).
Crosstalk in Cross-Hatched Ground Planes

When $Q$ is greater than 1, the circuit rings. When $Q$ is near 1, the circuit rise time follows Equation 5.6. For $Q$ less than 1, the circuit rise time is slower than Equation 5.6.

If a second trace close to the first trace also intersects the same slot, the two traces couple tightly together. The mutual inductance $L_M$ between it and the first trace is the same as $L$ in Equation 5.3.

If the second trace lies offset toward one end of the slot, its mutual inductance with the first trace decreases linearly with the distance between it and the slot's end.

The cross-coupling voltage between the two traces can be figured from knowledge of their mutual inductance and the rate of change in current in the driving circuit:

$$V_{\text{cross-talk}} = \frac{\Delta I}{10^{-90}} L_M$$

For a long line, the $\Delta I$ is just equal to the drive voltage divided by the characteristic impedance:

$$V_{\text{cross-talk}} = \frac{\Delta V}{10^{-90}} Z_0$$

For a short line driving a heavy capacitive load $C$, the rise time of change in current is a second derivative of voltage:

$$V_{\text{cross-talk}} = \frac{1.12 \Delta V C}{10^{-90}} L_M$$

Equations 5.4–5.10 apply equally well to inductance caused by any interruption in ground plane.

POINTS TO REMEMBER:

- Slots in a ground plane create unwanted inductance.
- Slot inductance slows down rising edges.
- Slot inductance creates mutual inductive crosstalk.

5.4 Crosstalk in Cross-Hatched Ground Planes

The power and ground grid diagrammed in Figure 5.10 saves board area, but at the expense of increased mutual inductance. This technique does not require separate power and ground plane layers. You may connect ordinary signals on the same layers as the power and ground connections. It is appropriate for small slow-speed CMOS and ordinary TTL designs but provides inadequate grounding for high-speed logic.
In the ground plane grid scheme, ground lines lie in a horizontal pattern on the bottom of a board, while power traces lie in a vertical pattern on the top. Connecting the two sets of line: at every intersection with a bypass capacitor makes a crosshatched pattern. Current return equally well to its source along either the ground or power wiring.

The bypass capacitors used in this system must be particularly good, as some returning current traverses several bypass capacitors on its way back to a driving gate.

The open pattern of power and ground traces leaves plenty of room for routing other signals on the power and ground layers. After completing power and ground connections, horizontal routing channels remain on the ground side and vertical routing channels remain on the power side of the board. If you must use two layer board, this is a good way to do it.

A related layout pattern is called cross-hatched ground plane. This pattern, entirely routed on one layer, consists of vertical and horizontal traces covering the board. The cross-hatched ground plane connects to ground. No other signals may be routed on this layer.

The cross-hatched ground helps implement high-impedance transmission structures on a thin board. Sometimes on a thin dielectric the narrow width required to implement satisfactory impedance is too small to fabricate reliably. In this case, a cross-hatched ground plane pattern etched into the ground layer adds series inductance and reduces shunt capacitance, thus raising the line's characteristic impedance. Don't try to implement controlled impedance lines on a cross-hatched ground plane unless tie lines run at 45 degrees to the hatch direction. The hatches must be much smaller than the length of a rising edge for this approach to work.

Both the power and ground grid and cross-hatched ground plane layouts induce a lot more mutual inductance between traces than solid ground planes. The question is, will your circuit work with that much mutual inductance?

First let's estimate the self-inductance of a single trace running across a cross-hatched ground plane. This estimation applies equally well to power and ground grid layout:

$$ L = \frac{L}{W} \ln \left( \frac{X}{W} \right) $$  \hspace{1cm} \text{[5.11]}

where $L =$ inductance nH

$X =$ hatch width, in.

$W =$ trace width, in.

$Y =$ trace length, in.

If the trace lies offset near one cross-hatched line, the inductance is a little less. Cross-hatched patterns that are as small or smaller than the width of a trace have almost no effect.

If a second trace, close to the first trace, runs between the same two cross-hatched members the two traces couple tightly together. The mutual inductance $L_m$ between it and the first trace is the same as $L$ in Equation 5.11.

If the second trace is offset by a good distance $D$, its mutual inductance with the first trace decreases with a denominator similar to Equation 5.2, but with the cross-hatched dimension $D$ replacing the term $H$.

$$ L_m = \frac{jY \ln(X/W)}{1 + (D/X)^2} $$  \hspace{1cm} \text{[5.12]}

Use the formulas from Section 5.3 for computing rise-time degradation and crosstalk voltage from this self-inductance and mutual inductance.

**POINT TO REMEMBER:**

If you must work with only two layers, use the power and ground grid system.

### 5.5 CROSSTALK WITH POWER AND GROUND FINGERS

The power and ground fingers layout, diagrammed in Figure 5.11, like the power and ground grid, allows some mutual inductive coupling but saves even more board area.
The old layout appears in old computer equipment (like the PDP-8) manufactured before the era of FCC-mandated radiation guidelines. The power and ground fingers layout is also used on cheap wire wrap frames. Don’t use it.

The power and ground fingers technique works only with very-low-speed logic implemented on small circuit cards. It’s main benefit is that the power and ground wiring can be implemented on a single layer. Signal traces require a second layer.

In the power and ground fingers scheme, one ground trace lies on the right side of the board and one power trace lies on the left. These traces extend from left to right when needed, like long fingers on rungs of a ladder.

Integrated-circuit packages stubble the runs, attached with short connections to ground or power traces. Bypass capacitors between adjacent power and ground wires complete the picture.

The problem with this layout is that most returning currents must go all the way around the edge of the board to get back to their driver. This diversion introduces massive amounts of self-inductance and mutual inductance.

If you must work with only two layers, use the power and ground grid approach in Section 5.4. If some unknown force compels you to use the ground fingers layout, first build up a sample board and measure the mutual inductance between traces. Then calculate whether your circuit has a chance of working. It might work with low-speed CMOS logic or with the old L3-TTL series, but not with any fast logic families. In addition to the danger of the produced simply not functioning, electromagnetic radiation from the open current loops will almost certainly null FPC radiation tests.

Here is an approximation for loop inductance in a power and ground fingers layout:

\[
L = 5Y' I \left( \frac{X}{W} \right)
\]

where \(L\) = inductance, \(I\) =
\(X\) = board width, \(W\) = trace width, \(Y\) = trace length.

Notice that doubling the trace width has almost no effect on the overall inductance. For ground traces do no help; what is needed is a web of smaller ground traces covering the surface of the board.

If a trace lies offset to one side, the inductance is a little less.

Because returning currents divert around the outside edge of the board magnetic fields are everywhere. Any second trace intersects these fields, coupling the traces tightly together. The mutual inductance \(L_m\) between any two traces is practically the same as \(L\) in Equation 5.13. There is not much of a decrease in mutual coupling with distance.

Use the formula: from Section 5.3 for computing rise-time degradation and crosstalk voltage from this self-inductance and mutual inductance.

**Pont to Remember:**

For high-speed logic, avoid the ground fingers layout.

### 5.6 Guard Traces

Guard traces appear extensively in analog design. At audio frequencies, on a two-layer board having no solid ground plane, a pair of grounded traces running parallel to a sensitive input circuit can reduce crosstalk by an order of magnitude.

In the digital world, a solid ground plane provides most of the benefits of grounded guard traces. Beyond the solid ground plane, guard traces provide little additional benefit. As a rule of thumb, the coupling between microstips is halved by inserting a third line, ground, at both ends, between them. Their coupling is halved yet again if the third line connect through vias to the other ground plane at frequent intervals. If you have

more than one ground plane layer, then ground the guard trace at each end, but not in the middle.

In digital problems, if two traces lie separated far enough to permit introduction of a guard trace, the coupling is usually already low enough that guarding is unnecessary. See Example 5.1.

**Example 5.1: Guard Trace Calculations**

Two traces, shown in Figure 5.12, lie separated by three trace widths. That is just enough room to fit in a guard trace.

![Guard Trace Positioning](image)

**Figure 5.12 Guard trace positioning.**

What is the estimated crosstalk?

Using Equation 5.1, the crosstalk fraction can’t be any worse than

\[ \text{Crosstalk} < \frac{1}{1 + (D/H)^2} \]

The centerline separation is 0.040, and the trace height is 0.005, so the ratio \( D/H \) is 8.

\[ \text{Crosstalk} < \frac{1}{1 - (8)^2} = 0.05 \]

This is not enough crosstalk to worry about in a digital system.

How much crosstalk is too much? In analog systems, high-powered signals which cross over to low-level inputs require very high crosstalk immunity. Heterogeneous digital systems that mix logic families are sensitive to crosstalk when higher voltage signals, like TTL, get near lower-voltage parts (like ECL).

For ordinary homogeneous digital systems, a crosstalk level of 1–3% between adjacent wires is fine. This assumes there exists a solid ground plane such that each wire interacts only with its nearest neighbors. Cross-coupling from other more remote wires is negligible. Using a shielded or fingered ground system, where many wire pairs interact, we must sum all the crosstalk contributions before arriving at the composite crosstalk level on a given signal.

Figure 5.13 illustrates a typical guard trace application. The driver sends a known voltage step down trace A. Crosstalk from this signal can be received on trace B or trace C. The traces are 26 in long, with a characteristic impedance of 50Ω.

![Guard Trace Demonstration](image)

**Figure 5.13 Guard trace demonstration.**

The various step responses for the system of microstrips appear in Figure 5.14. The large impulse is the crosstalk between wire A and B, with C left disconnected. The middle impulse is crosstalk from A to C, with B left disconnected. It is four times smaller than the A-to-B interference, as predicted by Equation 5.2. With trace B shorted to ground.
at both ends, we get the smallest coupling from A to C. This coupling is about one-half as big as the middle trace. This halving of coupling is the guard trace effect.

**POINT TO REMEMBER:**
- A solid-ground plane provides most of the benefit of grounded guard traces.

#### AR-END AND FAR-END CROSSTALK

The crosstalk examples in Sections 5.1-5.6 use lumped-circuit analysis. This simple mutual inductive coupling model works well for many coupling problems but no for long lines.

This section treats coupling between two long distributed transmission lines. Such coupling involves both mutual inductance and mutual capacitance.

##### 5.7.1 Inductive Coupling Mechanism

In this section we consider only the mutual inductive coupling. Section 5.7.2 discusses mutual capacitive coupling. J. L. Hart presents a somewhat more mathematical description of his same material.2

Figure 5.15 illustrates a typical crosstalk situation. The ends of his system are marked "near" and "far," as is common in the language of long-wire crosstalk.

Wire A-B carries a signal whose magnetic fields induce voltages in wire C-D. Magnetic coupling (mutual inductance) normally acts like a transformer. Because the mutual inductance is distributed, it appears as a succession of small transformers connected between the two lines.

Assuming the coupling is small (it had better be), the transformers do not significantly affect the propagation of signals from A to B.

As a voltage step moves from A to B, at each coupling transformer a small bip of interference appears on the adjoining line. Each bip propagates both forward and backward along line C-D.

For the moment, let's just consider the bip caused by transformer k. When a positive step arrives from A, the changing current induces a momentary voltage across transformer k, as shown in Figure 5.15. This voltage bip is the reaction of inductor L to a change in its current:

\[ L_\text{M} = \frac{dI}{dt} \quad [5.16] \]

The transformer reproduces this voltage bip on line C-D, with the polarity as marked. The interesting thing about mutual inductive coupling is that the polarity at each end of transformer k is different. A positive bip of voltage goes down line C-D to the left (reverse coupling), while a negative bip goes to the right (forward coupling).

The reflection diagram in Figure 5.16 shows the bip from all transformers added in a curious pattern. The negative (forward) bips all arrive together at the far end. The positive (reverse) bips arrive at different times, requiring a total of i/\omega_L to get to the near end.

Let's work with just the forward crosstalk coefficients for a moment. Each of the forward bips is proportional to the derivative of the input signal and to each mutual inductance L_M. Since all the forward bips arrive at the far end simultaneously, the total forward-bip size is proportional to the total mutual inductance between the two lines. If the lines were stretched longer, the total mutual inductance would increase and so would the forward mutual inductive crosstalk.

Reverse mutual inductive coupling is different. The total amount of coupling (total area) is the same as for forward coupling, but it spreads out over a period of 2\pi/\omega. If actual practice, all the reverse bip: smooth cut into one continuous blob of reverse coupling. The ideal reverse step response due to mutual inductive coupling is a rectangular function as shown in Figure 5.17.

I the line were stretched longer, the total mutual inductance would increase. The reverse coupling would respond by increasing its duration but not its height.

##### 5.7.2 Capacitive Coupling Mechanism

Distributed mutual capacitance works almost the same way is distributed mutual inductance. The difference lies in the polarity of couplings.

When a voltage step passes one of the mutual capacitors in Figure 5.15, a small bip of interference appears on the adjoining line. Each bip propagates both forward and backward along the line C-D.

![Figure 5.15 Mutual coupling between two long transmission lines.](image-url)

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Sec. 5.7 Near-end and Far-end Crosstalk

The polarities of mutual capacitive coupling are positive for forward and backward blips. Other than that, they behave the same as mutual inductive interference slips.

The mutual capacitance forward coupling looks like the derivative of the input signal. It gets larger for longer lines. Its polarity is positive (opposite of forward mutual inductive coupling).

The mutual capacitance reverse coupling area is the same as for forward coupling, but it spreads out over a period of $2T_p$. The ideal reverse step response due to mutual capacitive coupling is a rectangular function as shown in Figure 5.18.

5.7.3 Combining Mutual Inductive and Mutual Capacitive Coupling

Under normal conditions, over a solid ground plane, the inductive and capacitive crosstalk voltages are of roughly equal size. The forward crosstalk components (voltage at D) cancel, while backward crosstalk components (voltage at C) reinforce.

Stripeline circuits show particularly good balance between inductive and capacitive coupling and have tiny forward-coupling coefficients. Microstrips, for which the electric field lines responsible for crosstalk travel mostly through air instead of through the dielectric, have somewhat less capacitive crosstalk than inductive, leading to a small negative forward-coupling coefficient.

Over a slotted, hatched, or otherwise imperfect ground plane, the inductive crosstalk component is much larger than capacitive coupling and the forward crosstalk is large and negative. The forward crosstalk is never larger than the reverse crosstalk.
5.7.4 How Near-Enc Crosstalk Becomes a Far-end Problem

In Figure 5.15, the forward and reverse coupling signals are different. Each signal propagates to its respective end of cable C-D and terminates at the terminator.

Practical applications are often different from this model. In digital applications without source terminations, the device connected to the left end is Figure 5.9 is a low-impedance driver. Just like any other signal reverse crosstalk, when it hits this driver, reflects. The reflection coefficient for a low-impedance driver is almost -1. This changes the reverse coupling from positive polarity to negative polarity and sends it back toward the far end.

![Diagram of coupling](image1)

Reverse coupling which would appear if C were terminated in Z_o

Reverse coupling reflects off driver at C and appears at B, inverted, one transit time later.

Figure 5.19 Reverse coupling reflecting from a low-impedance driver.

The signal seen at the far end D is a copy of the reverse coupling signal at C delayed by the propagation time and inverted.

Because the mutual inductive and mutual capacitive portions of the forward coupling nearly cancel each other, the forward coupling is not visible when juxtaposed with this much larger reflected reverse coupling. When we measure crosstalk as defined by Figure 5.20, we are mostly measuring reflected reverse coupling.

**EXAMPLE 5.2: REFLECTED REVERSE CROSSTALK**

Figure 5.20 shows the measurement setup which produced the reflected reverse crosstalk waveforms in Figure 5.21.

The pulse generator drives trace A-B with a 2.5-V step input having a rise time of 800 ps. The waveform monitored at A appears in the top of Figure 5.21 at a scale of 1 V/division.

Figure 5.20 Setup for reflected reverse crosstalk measurement.

Figure 5.21 Reflected reverse crosstalk measurement.
Crosstalk signals at points D and F connect to regular coax probes and display in figures 5.21 at 50 mV/division. All probes are the same length. A1 probes terminate at the scope in 50Ω. The near ends of both pickup traces connect directly to ground, simulating a low-impedance driver.

Both crosstalk signals start together 4.5 ns after the initial rising edge:

\[ T = 4.5 \text{ ns} \]  \hspace{1cm} [517]

Both signals have a duration of 9 ns, and are of negative polarity.

Crosstalk duration = 2T = 9ns \hspace{1cm} [518]

The crosstalk signals measured at points D and F are:

\[ D = (2.5 \text{ divisions}) (10 \text{ mV/division}) = 125 \text{ mV} \] \hspace{1cm} [519]

\[ F = (0.7 \text{ division}) (5 \text{ mV/division}) = 35 \text{ mV} \] \hspace{1cm} [520]

The crosstalk ratios (output divided by input) measured for these two geometries are:

\[ \frac{D}{A} = \frac{0.125}{2.5} = 0.05 \] \hspace{1cm} [521]

\[ \frac{F}{A} = \frac{0.035}{2.5} = 0.014 \] \hspace{1cm} [522]

The crosstalk ratios predicted by equation 5.2 (K = 1) for these geometries are:

\[ \frac{E^+}{I} = \frac{1}{1 + (0.040 / 0.010)^2} = 0.059 \] \hspace{1cm} [523]

\[ \frac{E^-}{I} = \frac{1}{1 + (0.068 / 0.010)^2} = 0.015 \] \hspace{1cm} [524]

5.7.5 Characterizing Crosstalk Between Two Lines

Forward crosstalk is proportional to the derivative of the driving signal, and to line length. The constant of proportion depends on the balance between inductive and capacitive coupling. Once we measure this ratio for one known signal, modeling the response for other signals is trivial.

Modeling reverse crosstalk for fast rising edges is relatively simple. The reverse coupling looks like a square pulse, with rise and fall times comparable to the input signal amplitude. The reverse coupling percentage is a physical constant determined by the line parameters which is independent of line length. The duration of the pulse is 2T.

Reverse crosstalk for slow-rising edges is a little more involved. Once we have found the reverse coupling coefficient for fast edges, the reverse signal for any input can be found from

\[ \text{Reverse coupling} (i) = \alpha R \left[ V(t) - V(t - 2T) \right] \] \hspace{1cm} [525]

Sec. 5.7 Near-end and Far-end Crosstalk

where \( t \) = time, s
\( V(t) \) = driving waveform, V
\( \alpha R \) = reverse coupling coefficient for fast-edged signal
\( T_p \) = propagation delay of line, s

For lines longer than half the signal rise time, the reverse coupling has time to build up to its full value. The reverse coupling coefficient for such a line equals approximately

\[ \alpha R = \frac{1}{1 + (D/H)^2} \] \hspace{1cm} [526]

where \( D \) = separation between lines, in
\( H \) = line height above ground, in

For lines shorter than half the signal rise time the reverse coupling ramps up and then back down, never reaching its steady-state maximum value.

5.7.6 Using Series Terminations to Reduce Crosstalk

A series terminator extinguishes reverse-coupled crosstalk at the near end. An end terminator attenuates the returning reflection of the main signal, the reverse coupling from which would otherwise point toward the far end. Using both terminators eliminates both sources of reverse coupling noise, improving overall crosstalk considerably.

The reduced coupling gained by combining series and mid terminations lets us route parallel bus traces closer than would otherwise be practical.

**POINTS TO REMEMBER:**

Regarding long transmission lines:
- Over solid grounds, inductive and capacitive crosstalk are equal.
- Forward-crosstalk components cancel, while reverse crosstalk reinforces.
- Over a slotted or imperfect ground plane, the inductive coupling exceeds capacitive coupling, making forward crosstalk large and negative.

Forward crosstalk is proportional to the derivative of the input signal and to line length.

Reverse coupling looks like a square pulse, with a constant height and duration equal to \( T_p \). For short lines, reverse coupling does not climb to its full value.

Reverse crosstalk, when it hits a low-impedance driver, reflects toward the far end.
1 TO STACK PRINTED CIRCUIT BOARD LAYERS

A layer stack for a printed circuit board specifies the arrangement of circuit board layers. It specifies which layers are solid power and ground planes, the dielectric constant of the substrate and the spacings between layers. When planning a layer stack, also compute desired trace dimensions and minimum trace spacing.

Manufacturing constraints heavily influence the layer stack. As a rule, the greater the circuit wiring density, the greater your production costs per square inch. This section sets out some basic rules of thumb for planning layer stacks.

i.8.1 Power and Ground Planning

Design the power and ground layers first. To plan a power and ground system, first establish its design voltage levels, the number of signals, and the physical dimensions of the circuit board. Consider the physical dimensions, make a guess as to the trace width. The trace width assumption is not particularly critical at this stage.

Next estimate the self-inductance and mutual inductance using solid hatched, and fingers ground plane models. At this point it is usually clear which model suits the design. Remember that for the ground fingers mode, all traces interact. For the hatched model, traces running along the same hach grid intersect. For the ground plane model, only adjacent traces interact.

If you will be using a solid ground plane, plan on using ground and power planes in series. The symmetric pairing of solid planes in a layer stack helps prevent warping in the printed circuit board. A board with a single plane is offset to one side, car wax noticeably.

Power planes may be used as low-inductance signal return-current paths just as ground planes. Assuming adequate bypass capacitors between power and ground (Chapter 8), transmission lines routed over a power plane operate as well as those routed over a ground plane. Transmission lines routed between one power and one ground layer, or two power layers, also work.

3.8.2 Chassis Layer

Sometimes you will want to run a signal outside your digital system. For this application you may pick a low-speed or controlled-rise-time driver. This is a good choice because it reduces external radiation, which helps with FCC problems.

If the ground for the driver connects to ordinary digital logic ground, the effective driver output equals its intended drive voltage plus any noise voltage present on the digital logic ground. See Figure 5.12.

Digital logic grounds are notorious for high-frequency noise voltages. Grounds carry fluctuating voltages caused by the action of many returning signal currents acting across their self-inductance. These high-frequency fluctuations are too small to cause trouble in the digital circuits, but plenty large enough to exceed FCC limits. Any wire connected to the digital logic ground which runs outside the cabinet almost always fails FCC tests.

Without other precautions, the controlled rise-time driver effectively picks up ground noise and broadcasts it outside the chassis.

sec. 5.8 How o Stack Printed Circuit Board Layers

A ground connection at high frequencies between logic ground and true earth ground may be ineffective.

Figure 5.22 Using a controlled-rise-time drive.

One solution to this problem adds a chassis plane to the layer stack. This plane stacks directly next to a ground plane, giving a very tight capacitive coupling between the two planes. At high frequencies, the two planes are effectively tied together. The chassis plane helps to reduce, solder, or weld to the extended chassis along one continuous axis near the controlled-rise-time driver. At high frequencies, we have effectively shorted the digital ground plane to the chassis. This reduces the amount of digital ground noise at that point, also reducing noise carried by the controlled-rise-time driver to the outside world.

Ordinary capacitors will not function as a short between chassis and digital logic ground, because they have too much lead inductance. Only the large, wide, parallel surfaces between the chassis plane and digital ground plane have a low enough inductance to effectively short the two together.

With the chassis plane approach, the digital logic and external chassis remain electrically isolated at low frequencies. This may be desirable for safety or other reasons. If the isolation does not matter, simply short digital logic ground directly to the chassis without using a separate chassis layer. Make this connection by screwing, soldering or welding the ground plane to the external chassis along one continuous axis near the controlled-rise-time driver.

When using a chassis plane, counterbalance its in the layer stack with some other solid plane layer. For mechanical reasons always lean toward using symmetric arrangements of planes in your layer stack.

5.8.3 Selecting Trace Dimensions

Squeezing traces tightly together increases the circuit packing density. Very dense designs require fewer circuit board layers. Since printed circuit board costs are proportional to the number of layers, as well as to the board surface area, we are tempted to always design using the fewest number of layers that will do the job.
Smaller, more closely spaced traces also yield more crosstalk and less power-handling capacity. This tradeoff among crosstalk, routing density, and power is critical to low-cost product design.

Let's deal with power-handling capacity first, because it is the simplest of the constraints.

The power-handling capacity of a printed circuit trace depends mostly on its cross-sectional area and the allowable temperature rise. For a given cross-sectional area, a trace's temperature rise above ambient is roughly proportional to the power it dissipates. Large temperature rises are unreliable and heat up nearby digital circuits. A conservative upper limit on trace heating inside digital products is 10°C.

Figure 5.23 relates maximum power-handling capacity to temperature rise. The horizontal axis in Figure 5.23 measures cross-sectional area in units of square inches. The vertical axis of Figure 5.23 shows the allowable current for that trace at a given temperature rise.

For example, a 0.010-in.-wide trace of 1-oz copper (0.0015 in. thick) can safely pass 750 mA at a temperature rise of 10°C.

Power is rarely a serious constraint except for large power distribution buses. As thin-film technology, with extremely small trace cross sections, becomes more widely available, heating limitations may become more prevalent.

A second lower bound on trace width results from the manufacturing process. Table 5.1 lists the minimum trace widths attainable in various production processes.

![Image: Temperature rise vs. current capacity diagram]

**Figure 5.23** Current-carrying capacity of copper printed circuit traces.

*Example: A trace 0.010 in. wide, fabricated from a 1-oz-weight copper (0.00135 thickness), has a cross-sectional area of $1.35 \times 10^{-3}$ in.$^2$."

### Table 5.1 Minimum Line Widths Attainable with Various Production Processes

<table>
<thead>
<tr>
<th>Process</th>
<th>Minimum line width (in.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gold-soldered onto thick film substrate</td>
<td>0.01</td>
</tr>
<tr>
<td>Etched copper on epoxy board with plating</td>
<td>0.04</td>
</tr>
<tr>
<td>Etched copper on epoxy board with no plating</td>
<td>0.03</td>
</tr>
<tr>
<td>Gold-evaporated onto thin film substrate</td>
<td>0.01</td>
</tr>
</tbody>
</table>

With any process the manufacturing yield will drop, and cost will go up, as one approaches the minimum attainable trace width. This factor prevents most designers from using the minimum attainable line width.

Other factors tend to increase line width. Poor control over the etching process can result in large line width variations. At low line widths, the percentage line width variation, which controls the percentage impedance tolerance, may be unacceptable. A need for accurate impedance control can force the use of lines much wider than the minimum attainable trace width.

Use the formulas for trace impedance in Appendix C to find a combination of trace width and height sufficient large that, over expected variations in width and layer height, the impedance stays within your design range. Remember that you must also allot room in your impedance budget for variations in the effective permittivity of the substrate.

Consideration of power, cost, and impedance tolerance usually drive the selection of a particular trace width. Given the width, the impedance constraint sets the layer height.

Next, using the formula for crosstalk (see Section 5.7.3 and Equation 5.2), figure the minimum spacing between adjacent traces (center to center). This number is called the minimum trace pitch. The unused distance between traces is called the trace separation. The sum of the trace separation and the trace width equals the trace pitch.

**Points to Remember:**

As a rule, the greater your circuit wiring density the greater your production costs per square inch.

*Printed circuit board cost is proportional to the number of layers and to the board surface area.*

*Design the power and ground layers first.*

*For mechanical reasons, lay toward using a symmetric arrangement of ground and power planes in your layer stack.*

*Smaller, more closely spaced traces yield more crosstalk.*
58.4 Routing Density Versus Number of Routing Layers

With more layers, we can spread the traces out farther, that makes routing easier and reduces the risk of crosstalk problems. Unfortunately, the cost of multilayer printed circuit boards is proportional to the number of layers times the surface area. Using more layers costs more.

With fewer layers, we must use a narrower trace pitch, which can also cost extra. Not only that, at a fine enough pitch we run the risk of too much crosstalk.

Determining the best cost number of layers for a board is a matter of experience and guesswork. The central issue involves estimating the trace pitch required to route $N$ connections on a certain-size board, using $M$ layers. Knowing the trace pitch, we can find out how much the board will cost and at the same time model the crosstalk.

Trace pitch is determined from wiring density. One useful model for wiring density is called Rent's rule, after the IBM engineer who popularized it. Rent noticed that most large square boards, when divided into quadrants, reveal half their wiring going between quadrants and half staying within each quadrant. Further subdividing of each quadrant, reveals the same distribution. If, upon traveling between two quadrants, we assume (this is very hypothetical) a wiring length is average equal to the spacing between quadrants, we arrive at a total average wiring length equal to three-eighths of a board size.

Knowing the average wire length and the number of wires we can compute the total board surface area occupied by these wires using any trace pitch. This knowledge, in the form of Equation 5.27, shows the trace pitch required to route $N$ connections on a fixed-size board using $M$ layers.

Of course, if we have some other information about the routing requirements, such as large buses or other structures, we should use that. Given no other information, we can attempt to calculate the required trace spacing on a board using Rent's idea:

$$P_{ave} = \frac{(XY)^{N}}{N} = 2.7M$$ (5.27)

where $N$ = number of connections (assumed distributed according to Rent's rule)

$P_{ave}$ = average trace pitch, in.

$X$ = board width, in.

$Y$ = board height, in.

$M$ = number of routing layers

For example, on an 8 in. x 12 in. board having 800 interconnections routed on four layers, we need a trace pitch, on average, of 0.132 in. This means that if the board is pretty much covered with DIP through-holes, we will need one trace routed between almost every pin.

Don't count on filling more than half the spaces between pins. In the above example we should plan on more layers or plan on using double-trace routing (two traces between each pin).

Sec. 5.8 How to Stack Printed Circuit Board Layers

For through-holeboards, the average pitch predicted by Equation 5.27 and the minimum pitch required are very different. Use the minimum pitch determined from crosstalk considerations to determine if you need double- or triple-track routing between pins. Use the average pitch predicted by Equation 5.27 to determine how many available routing tracks we need.

Inner layers of surface-mounted boards may have more routing space available than DIP boards. The total number of via's is roughly the same, but the vias are smaller in surface-mount designs since IC pins don't have to stick through them. The average and minimum pitch for inner layers of surface-mount boards may be similar.

Routing up to four tracks between pins is possible on inner layers of epoxy circuit boards, but this may lead to severe crosstalk problems.

Extra routing space on a board can be gained by leaving large spaces between cups, but this takes more total surface area. Most designers choose to go with more layers instead.

If crosstalk is a problem, ensure that the layout squeezes traces together only to fit between pins and then immediately spreads them back out again on their way to the next cup. This requires a lot of hand adjustment, but even modest increases in trace separation reduce crosstalk.

With any luck, we can find some number of circuit board routing layers that yield acceptable crosstalk and won't cost too much.

POINTS TO REMEMBER:

Don’t count on filling more than half the spaces between through-hole pins.

When all else fails, use Rent’s reasoning to figure the average trace length.

58.5 Classic Layer Stacks

Figures 5.2-5.26 illustrate three classic layout stacks for 4, 6, and 10 layers. These stacks are designed for use with the ordinary epoxy multilayer fabrication process described below. Beyond 10 layers, designers usually incorporate additional ground planes to isolate sets of routing layers.

These stacks are appropriate for high-speed computer products embedded within well-shielded card cages. If you are planning systems that must pass FCC, VDE, Tempest, or other mandated rules for electromagnetic emissions without the benefit of a well-shielded card cage, these simple stacks will be inadequate for your purposes.

In each figure, the terms horizontal routing and vertical routing refer to the orientation of traces on that layer (horizontal or vertical). Traces on each layer traditionally lie
parallel to each other, with every other layer built at right angles to the one below it. Very few traces cut diagonally across any layer or make large 90-degree bends. This increases the routing efficiency.

Power and ground layers in Figures 5.24–5.26 are marked with thick solid lines. Trace layers show the proportional line width and trace height.

The notations core and prepreg refer to materials used in the substrate laminating process. The following paragraphs briefly describe one commonly used process for building circuit cards. If you want to tightly control trace-to-ground spacings, you need to know about core and prepreg layers.

The multilayer buildup process starts with a stack of raw two-sided laminate layers coated with copper on each side. Surfaces destined to become inner layers are etched in this form. Surfaces destined to become outer layers are left full copper-pated. These etched laminates are called cores. The thickness between opposing layers on a core depends on the thickness of the original laminate.

The cores are then stacked together with a sheet of prepreg epoxy material placed between each pair of cores. This sheet melts into an epoxy glue when heated and pressed. The thickness of the prepreg sheet determines the spacing between core layers. The prepreg cures into a hard epoxy layer having the same dielectric constant as the core layers. Core and prepreg layers alternate.

Figure 5.24 Four-layer stack.

Figure 5.25 Six-layer stack.

Because the prepreg partially melts in the process, traces on opposite sides of the prepreg tend to sink into the melted, gluey prepreg material. Accurate analysis of trace-to-ground separation takes into account the fact that the spacing between facing sides of two traces on either side of a prepreg layer will be reduced by twice the trace thickness as they sink into the prepreg.

Manufacturers sometimes form the outer layer from one side of a core and in other cases they form it from a metal foil pressed onto a toplayer of prepreg. In either case, the outer layer is a solid copper sheet. (No etching yet.)

After the prepreg cures, holes are drilled through the assembly. The drilling exposes the various copper layers and pads which it penetrates in the inner layers, but they are at this point not connected electrically.
### Points to Remember:

Core and prepreg layers alternate.

Outer layers, if slated, have greater trace width variation than inner traces.

Traces on routing layers tend to sink into the prepreg mixture. Their thickness doesn't add to the total board thickness.

The thickness of solid ground plane layers always adds to the total board thickness.

### 5.8.6 Extra Hints for High-speed Boards

For the very highest-speed boards, place power and ground layers directly together. This positioning maximizes their capacitive coupling, reducing power supply noise.

Use plenty of extra ground planes (not power planes) to isolate sets of routing layers. Sprinkle around lots of ground vias, connecting together the many ground planes. Returning signal currents will flow through these ground vias as they jump from layer to layer following the contorted path of each signal trace.

Had we used a mix of power and ground planes for isolating routing layers, instead of just ground planes, the return currents, which always flow in the nearest plane, would have had to traverse many bypass capacitors as they jumped between ground and power planes. This is not a good idea, because any currents we send through the bypass capacitors will cause voltages across them. These voltages radiate very effectively from the power and ground planes, adding to our radiated noise problems.

### Points to Remember:

At the highest speeds, keep ground and power planes directly adjacent.

Use extra ground planes, not power planes, to isolate routing layers.