

portable among different logic families, than direct voltage readings. The *noise margin percentage* is equal to the lesser of

$$\frac{V_{OH \text{ min}} - V_{IH}}{V_{OH \text{ max}} - V_{OL \text{ min}}} \quad \text{or} \quad \frac{V_{IL} - V_{OL \text{ max}}}{V_{OH \text{ max}} - V_{OL \text{ min}}} \quad [2.45]$$

The noise margin percentage of 10KH ECL logic is 17.8%, while 74AS TTL logic has a margin of only 9.1%. This difference is the basis for claims that ECL logic has better noise immunity than TTL. While the actual margin voltages for ECL are smaller than for TTL, they are a bigger percentage of the ECL voltage swing.

Of course, the 10KH family switches two to three times faster than the 74AS family. Faster switching time increases return-current problems, crosstalk, and ringing. Overall it is more difficult to control return current, crosstalk, and ringing with the MC10KH family than with the 74AS, but not two to three times harder.

POINTS TO REMEMBER:

Given two logic families with identical maximum propagation delay statistics, the family with the slowest output switching time will be cheaper and easier to use.

We can figure the dl/dt in an output circuit given the voltage rise time and the load.

When we halve the rise time, we quadruple the amount of dl/dt flowing into capacitive loads.

A complete voltage margin budget in a system accounts for the effects of power supply variations, ground shifts, signal crosstalk, ringing, and thermal differences.

2.4 PACKAGING

Variety in packaging springs from the same well that sustains so many different circuit configurations. The number of logic packaging schemes is enormous and growing daily.

Almost all packages, when used at high speeds, suffer from problems with lead inductance, lead capacitance, and heat dissipation.

2.4.1 Lead Inductance

The inductance of individual leads in a device package creates a problem called *ground bounce*. This phenomenon causes glitches in the logic inputs whenever the device outputs switch from one state to another. The magnitude of these glitches, and the effects they cause, are the subject of this section.

2.4.1.1 Unwanted Voltages on Ground Wires—Why Ground Bounce Occurs

Figure 2.16 represents an idealized logic die, wire-bonded to four pins of a DIP package. One transmit circuit and one receive circuit are shown. The transmit circuit shown is a totem-pole output stage, although any configuration exhibits the same problem at high speeds.

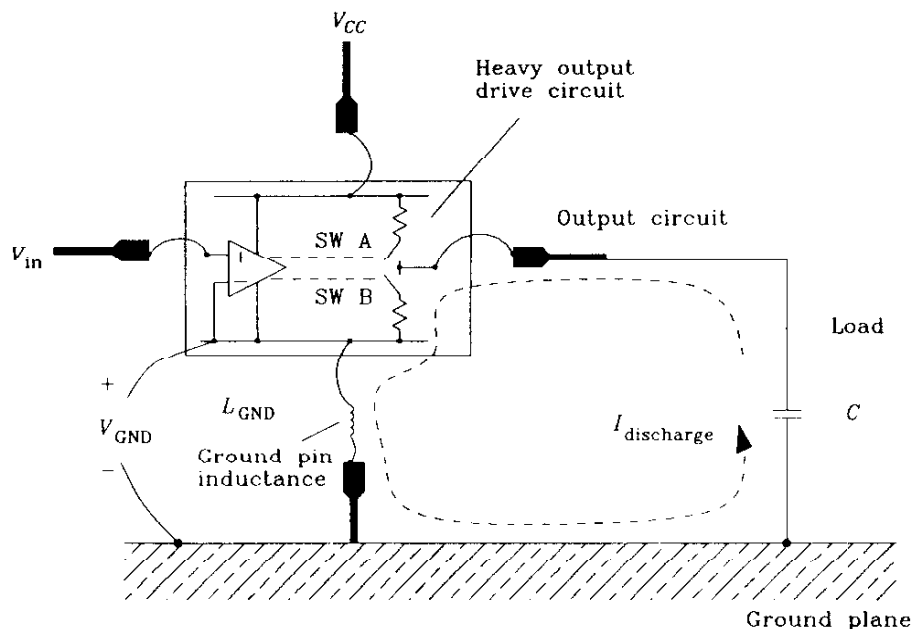
Suppose switch B of the output driver has just closed, discharging load capacitor C to ground. As the voltage across capacitor C falls, its stored charge flows back to ground, causing a massive current surge around the ground loop shown as $I_{\text{discharge}}$.

As the discharge current builds and then recedes, changes in that current, working across the inductance of the ground pin, induce a voltage V_{GND} between the system ground plane underneath the device and the ground internal to the package. The magnitude of this voltage is equal to

$$V_{\text{GND}} = L_{\text{GND}} \frac{d}{dt} I_{\text{discharge}} \tag{2.46}$$

Shifts in the internal ground reference voltage due to output switching are called *ground bounce*.

The ground bounce voltage V_{GND} is usually small compared to the full-swing output voltage. It does not act to significantly impair the transmitted signal, but it interferes in a major way with reception.



$$V_{\text{GND}} = L_{\text{GND}} \frac{d}{dt} (I_{\text{discharge}})$$

Figure 2.16 Lead inductance of a logic device package.

Consider the receiver section of the same die. This receiver differentially compares the input voltage V_{in} against its local internal ground reference.¹⁴ This differencing operation appears in Figure 2.16 as a plus (+) input connected to V_{in} and a minus (-) input connected to the internal ground. Because the internal ground carries the V_{GND} noise pulse, the actual differential voltage seen by the input circuit is equal to

$$\text{Input circuit sees: } V_{in} - V_{GND} \quad [2.47]$$

Because the input circuit responds to the difference between its plus (+) and minus (-) inputs, it has no way of knowing whether the noise pulse V_{GND} has been added to the minus (-) input or subtracted from the plus (+) input. In other words, the V_{GND} pulse looks to the inputs circuit like noise directly superimposed on the input signal.

If we simultaneously switch N outputs from a chip into N corresponding capacitive loads, we get N times as much ground current and the pulse V_{GND} looms N times larger.

Ground bounce voltages are proportional to the rate of change in current through the ground pin. When driving capacitive loads, we expect the rate of change in current to look like the second derivative of the voltage. Referring to Figure 2.14, the second derivative of the voltage is a double-humped waveform, first bumping up, and then bumping down.

2.4.1.2 How Ground Bounce Affects Your Circuit

Figure 2.17 illustrates a ground bounce situation. Imagine a TTL octal D flip-flop, with a single clock input, driving a bank of 32 memory chips. At 5 pF per input, each address line is loaded with 160 pF.

Suppose data comes into the D input with plenty of setup time but with little hold time. Figure 2.17 illustrates data arriving with a 3-ns setup time and a 1-ns hold time. Assume this timing meets the requirements of our octal TTL flip-flop.

On clock edge A the flip-flop latches in data word FF hex. At clock edge B the flip-flop latches in data 00 hex. In both cases, the flip-flop propagation delay of 3 ns is slightly longer than the required hold time.

At point C , let the input data change to any pattern XX. Point C follows 1 ns after clock pulse B . At this point, the flip-flop has internally latched in the 00 data word, but the Q outputs have not yet switched from FF to 00.

The next to the bottom trace shows V_{GND} . After point A , when the Q outputs switch positive, the load-charging current flows in the V_{CC} pin, not the ground pin, so we get little noise on V_{GND} . At point D all eight outputs swing LO, and we get a big V_{GND} noise pulse. This noise pulse causes an error called *double-clocking*.

Double-clocking results from differential input action in the clock circuit. Internal to the flip-flop, the clock input measures the difference between the chip's clock pin and its ground pin. The bottom trace of Figure 2.17 shows this difference. The difference

¹⁴This is representative of TTL circuits. CMOS circuits tend to compare inputs against a weighted average of V_{CC} and ground. ECL and the 10G GaAs family compare inputs against V_{CC} . In all cases, the same effect applies, with slightly different topology.

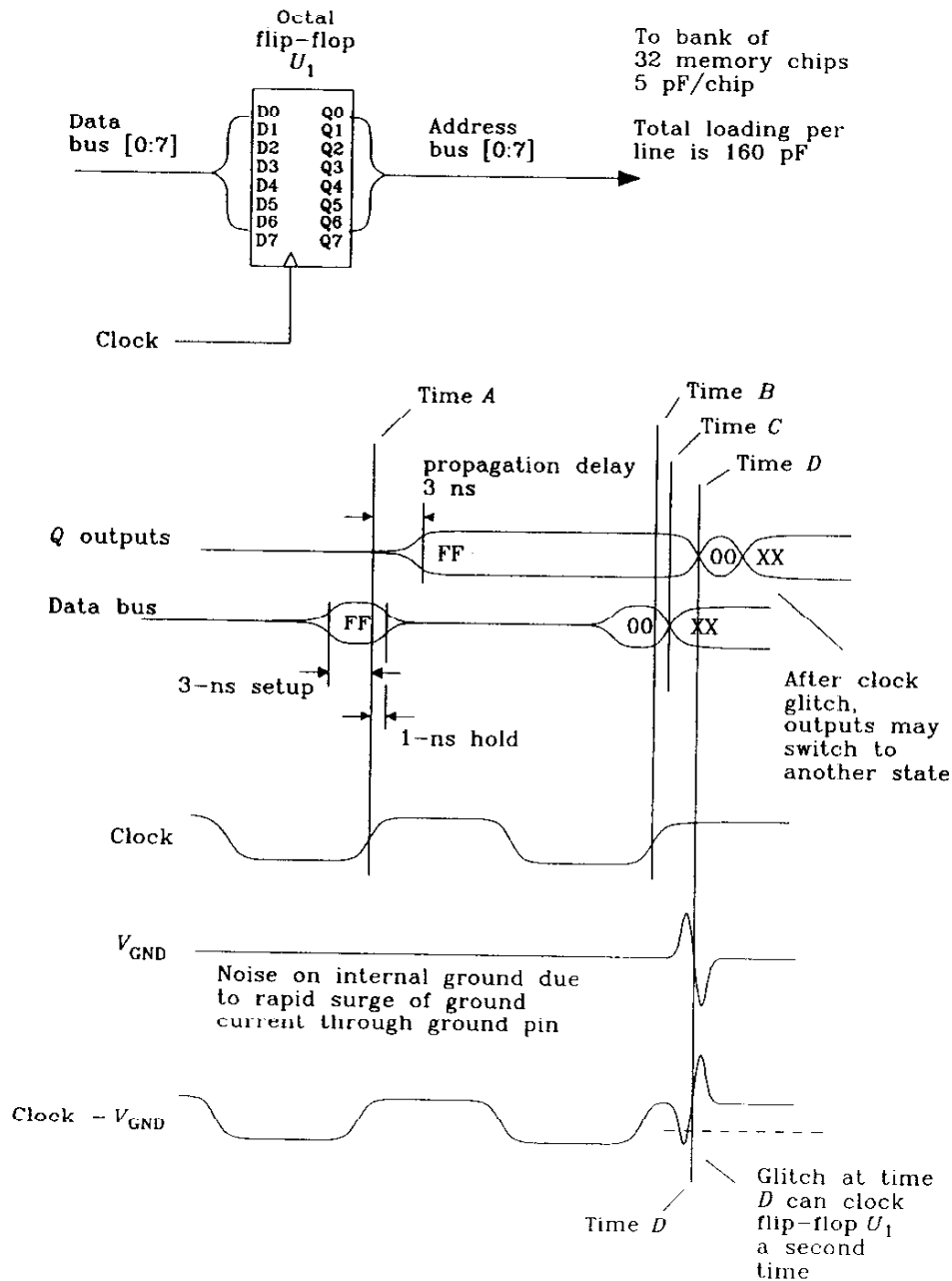


Figure 2.17 Example of ground bounce.

waveform has a clean clock edge at B, followed by a big glitch induced by signal currents flowing in the ground pin. The flip-flop will relock itself on this pulse.

If the data input has changed by the time the second clock at D happens, the flip-flop will proceed ignorantly to state XX. The Q outputs at point D momentarily flip to the correct state and then mysteriously flip to some wrong condition.

External observations of the clock input show a perfectly clean signal; it is only internal to the logic package that anything is amiss.

The double-clocking error happens on DIP flip-flop packages which have very fast output drivers connected to heavy capacitive loads. Large latches in the FCT family, sold in a DIP package, have exhibited this problem. Surface-mounted packages, with their shorter pins, are less susceptible to double-clocking. As new generations of flip-flops get faster, we will need new packages with less and less ground inductance to house them.

Providing special power pins for the output drivers separate from those used for referencing input signals elegantly circumvents the ground bounce problem. Since little current flows in the input ground reference pins, no ground bounce effect occurs. Most ECL families, and many gate arrays, use separate power pins for this purpose.

Edge-sensitive input lines such as resets and interrupt service lines are particularly susceptible to ground bounce glitches.

2.4.1.3 Magnitude of Ground Bounce

Let's look at a concrete example to see how big the ground bounce pulse can be.

EXAMPLE 2.6: Measurement of Ground Bounce

For this measurement we will use a quad flip-flop, configured so that three of its outputs are toggling while the fourth output stays fixed at zero. We have the ability to switch 20-pF loads onto any of the three active outputs. This experimental arrangement can show ground bounce with no load or with heavy loads.

Because the inactive fourth output stays at logic LO, it serves as a window into the chip through which we may measure the internal ground voltage.

Figure 2.18 shows the arrangement. The clock and asynchronous reset lines alternately set and reset the three active outputs. For this experiment we use a 74HC174 flip-flop.

With all three loads connected we get the waveforms in Figure 2.19. When the Q outputs switch HI, there is a small V_{GND} glitch. This corresponds to switching currents internal to the device (see Section 2.2.2). When the Q outputs switch LO, the big ground bounce pulse appears. In this example it is about 150 mV tall.

A pulse of only 150 mV may not seem like much, but consider these facts:

- (1) The low-side voltage margin on HCT logic is only 470 mV.
- (2) If we had eight simultaneous outputs switching, the pulse would be eight-thirds times bigger.
- (3) Ground bounce reduces the available residual noise margin used to compensate for other noise and signal distortion effects.

Identical measurements carried out on a 74F174 flip-flop result in a ground bounce of 400 mV.

2.4.1.4 Predicting Ground Bounce Magnitude

To make useful predictions about ground bounce we need to know four facts: The 10–90% switching time of the logic device, the load capacitance or resistance, the lead inductance, and the switching voltage.

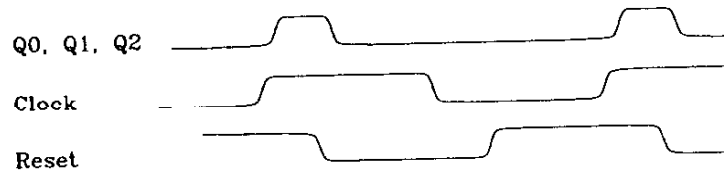
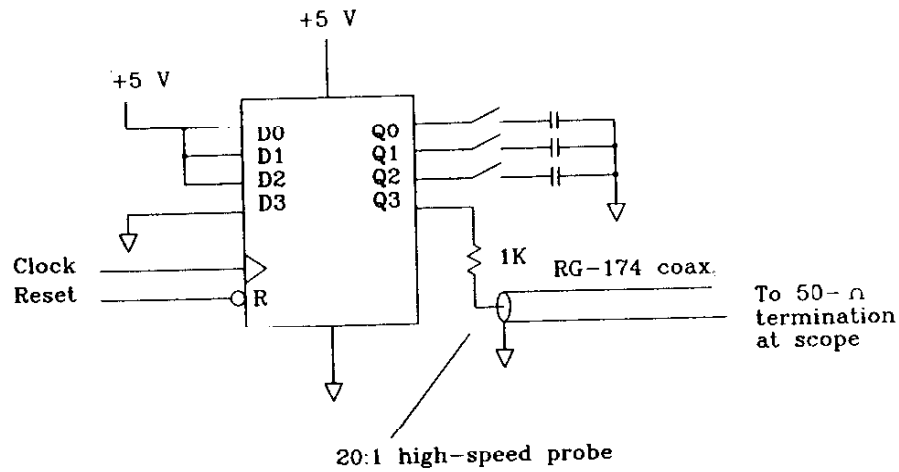


Figure 2.18 Measuring ground bounce.

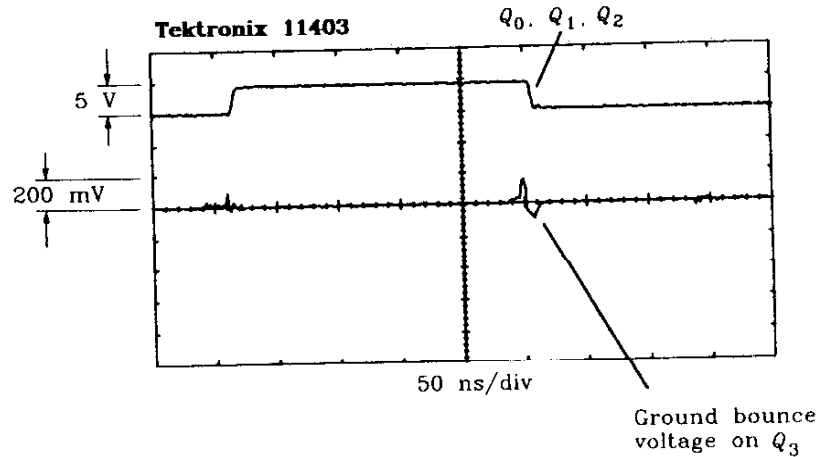


Figure 2.19 Ground bounce on 74HC174 with three loads of 20 pF.

For a resistive load R , we can use Equation 2.41 to find the rate of change in current and then the definition of inductance (Equation 1.17) to compute the ground bounce amplitude:

$$|V_{GND}| = L \frac{\Delta V}{T_{10-90}} \frac{1}{R} \quad [2.48]$$

For a capacitive load C , we can use Equation 2.42 to find the rate of change in current and then the definition of inductance (Equation 1.17) to compute the ground bounce amplitude:

$$|V_{GND}| = L \frac{1.52 \Delta V}{T_{10-90}^2} C \quad [2.49]$$

The factors ΔV and T_{10-90} depend on the logic family. Here are typical figures.

Table 2.2 compares the switching characteristics of five logic families: Signetics 74HCT CMOS, Texas Instruments 74AS TTL, Motorola 10KH ECL, GigaBit Logic 10G GaAs, and NEL GaAs.¹⁵

TABLE 2.2 SWITCHING CHARACTERISTICS OF FIVE LOGIC FAMILIES

	74HCT CMOS	74AS TTL	10KH ECL	10G GaAs	NEL GaAs
ΔV_{max} (V)	5	3.7	1.1	1.5	1.0
T_{10-90} (ns)	4.7	1.7	0.7	0.15	0.05

Ground lead inductance is a strong function of the package type. Larger packages have more lead inductance. Packages with internal ground planes do better but do not eliminate the ground bounce problem. Wide, low-inductance internal ground plane structures still have skinny leads connecting the internal ground plane to external ground.

The most promising techniques for dramatically reducing lead inductance are wire bond, tape automated bonding (TAB), and flip-chip. All three techniques shorten the ground wire connections between the chip and its printed circuit board. See Figure 2.20. For an excellent overview of modern packaging techniques, see footnote.¹⁶

The wire bond method places an unsealed die on its back on a printed circuit board and welds tiny bonding wires between the chip pads and the printed circuit board. The chip and its wire bonds are then sealed with a blob of coating material or covered with a hermetically sealed lid over the entire circuit board.

Wire bonding is a mechanically simple method with plenty of tolerance for changes in either the chip bonding pad locations or printed circuit board wiring. Wire bonding can be done by hand for very low-volume applications.

Tape automated bonding replaces the wire bonds with a mass termination technique. Interconnecting wiring used to connect the chip to a printed circuit board is first printed on a very thin flexible substrate (a flex circuit). This substrate may have more than one layer, including a ground layer for impedance control. Solder bumps are then placed on the chip bonding pads, and the chip reflow-soldered to the flex circuit. The chip now has the flex circuit bonded to its face. As a second step, the combination chip and flex circuit is reflow-soldered to the printed circuit board. The result is then sealed with a blob of coating material or covered with a hermetically sealed lid over the entire circuit board.

¹⁵At the time of writing, NEL holds the record among commercially available digital logic families for switching speed. For more information contact KBK, Inc., New York, New York.

¹⁶H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*, Addison Wesley, Reading, Mass., 1990.

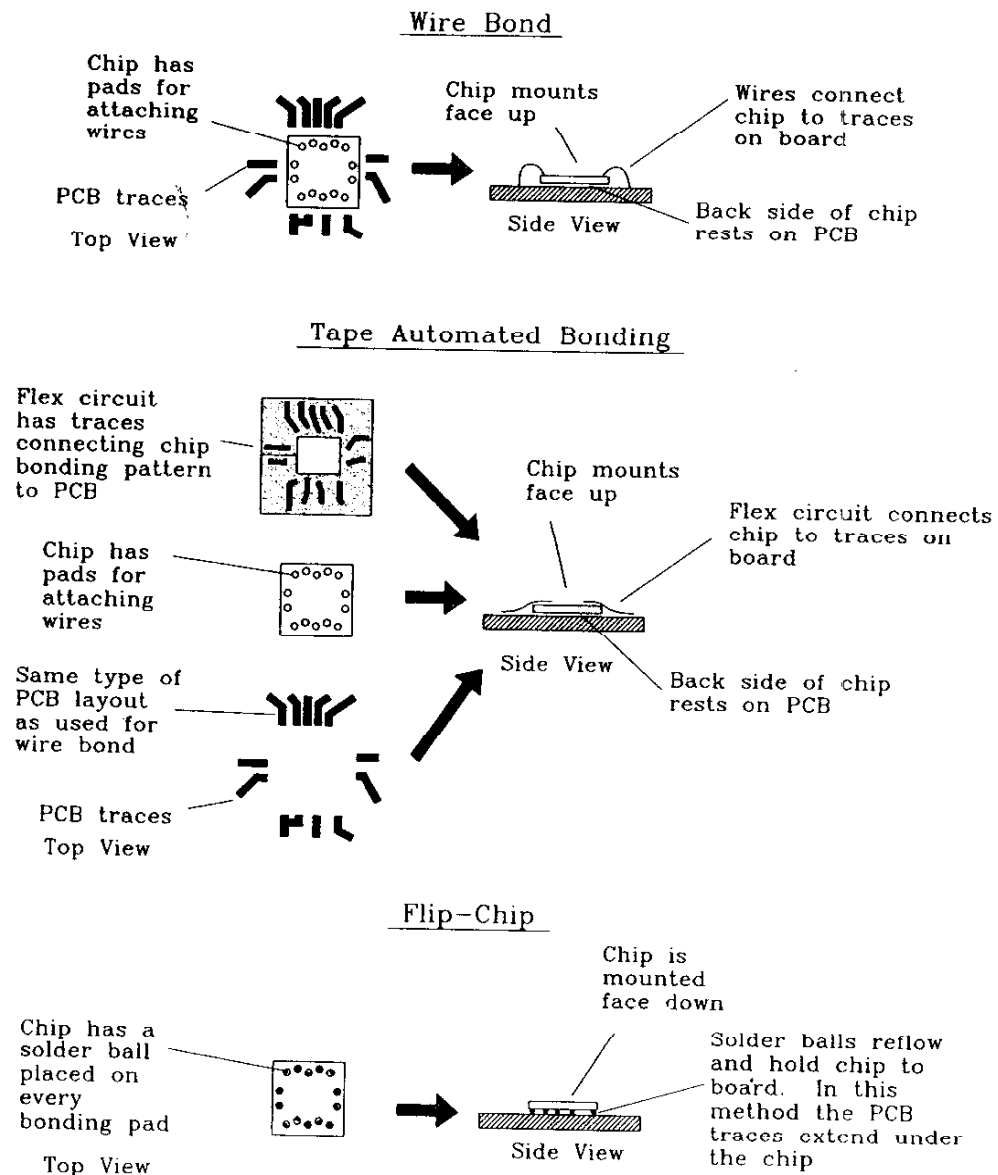


Figure 2.20 Methods of direct chip attachment.

Tape automated bonding, being a mass attachment technique, is very quick. It has the advantages of providing a continuous ground plane for all signals and also providing some mechanical compliance between the chip and printed circuit board. TAB can accommodate lead spacings as small as 0.08 mm (300 leads/in.). The disadvantages of TAB are that a different flex circuit is needed for each chip and that the flex circuit must change if either the printed circuit board or chip bonding patterns change.

Flip-chip technology first places solder balls on each chip attachment pad. The chip is then turned face down onto the printed circuit board and directly reflow-soldered in place. Flip-chip mounting is often used on ceramic multichip modules which incor-

porate advanced cooling structures and an overall hermetic seal around the entire enclosure.

Electrically, flip-chip technology is ideal. The bonding lengths are miniscule, and so all parasitics associated with packaging are minimized. Mechanically and thermally, flip-chip technology is miserable. There is no mechanical compliance between chip and printed circuit board except the limited springiness of the solder balls themselves. The thermal coefficient of expansion between the chip and printed circuit board must match extremely closely.

Cooling difficulties are exacerbated with the flip-chip method because the chip substrate is held up off the printed circuit board. In both the wire bond and TAB methods the chip mounts with its back side touching (often glued to) the printed circuit board which provides a good conduit for heat dissipation.

Table 2.3 lists typical lead inductance figures for various packages.

TABLE 2.3 LEAD INDUCTANCE OF LOGIC PACKAGES*

14-pin plastic dual in-line package (DIP)	8 nH
68-pin plastic DIP	35 nH
68-pin surface-mount plastic leaded chip carrier (PLCC)	7 nH
Wire bonded to hybrid substrate	1 nH
Solder bump to hybrid substrate	0.1 nH

*Much of this data is taken from H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*, Addison Wesley, Reading, Mass., 1990, Table 6.2. Reprinted by permission of Addison-Wesley Publishing Co., Inc., Reading, MA.

2.4.1.5 Factors that Reduce Ground Bounce

Slowing down the output switching time is a good idea. The 10K ECL family, the CMOS FCT family, and a few newer bus drivers incorporate circuitry designed to slow down the edge transition time with minimal impact on overall propagation delay.

Some manufacturers put multiple ground wires on their packages. This is a good idea if the grounds are spaced evenly around the die. If the grounds are all near each other, going from one to two grounds nearly halves the ground inductance, but increasing the number of nearby grounds beyond two has a diminishing effect. Spreading the grounds out evenly around the chip is much better than lumping them together.

Components which bring out a separate ground reference pin for the input circuitry attack the problem in a more subtle way. These circuits, like the 10K family, provide a separate sense wire for the internal reference voltage generator which has a direct path to the external ground. This pin does not carry large ground currents and subsequently acquires no ground bounce. This is an excellent method of attacking ground bounce problems. For chips with separated grounds, make sure each ground wire has a direct path to the ground plane. Connecting the two grounds together and then running them through a trace to ground defeats the purpose of having independent ground leads.

Differential inputs are a similar and even more effective means of achieving the same end.